# ISOFACE™

# ISO1I813T

Isolated 8 Channel Digital Input with IEC61131-2 Type 1/2/3 Characteristics

## Data Sheet

V 2.1, 2015-05-22

Power Management & Multimarket

**Edition 2015-05-22**

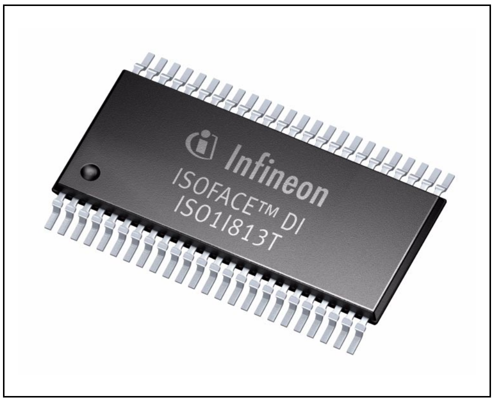
**Published by**
**Infineon Technologies AG**
**81726 Munich, Germany**

**Revision History: 2015-05-22, V 2.1**

**Previous Version: Data Sheet V2.0**

| Page | Subjects (major changes since last revision) |
|---|---|
| V 2.1 | Data Sheet |
| 48,55 | Typo inside register adress for GLCFG corrected |
| V 2.0 | Data Sheet |
| 6, 9, 11 | Description of SEL pin corrected |
| 24 | Chapter 3.6 Programmable Digital Input Filter updated and information about filter times added |
| 26 | Chapter 3.7 Parallel Interface Mode updated |
| 29 | Chapter 3.8.1 SPI Modes write access decription updated |
| 34 | Chapter 3.9 SYNC Operation updated |
| 35 | Chapter 3.10 Write-Read- Access and Read-Read-Access for Different Applications added |
| 37 | Table 3 System Insulation Characteristics Condition for Production test added |
| 45 | Table 15 Parallel Interface timing updated |
| 46 | Table 16 Serial Interface timing updated |

# Isolated 8 Channel Digital Input with IEC61131-2 Type 1/2/3 Characteristics




## Product Highlights

- **Minimization of power dissipation due to constant current characteristic**
- **Status LED output for each input**
- **Digital averaging of the input signals to suppress interference pulses**
- **Isolation between Input and Output using Coreless Transformer Technology**

### Features

- Complete system integration (digital sensor or switch input, galvanic isolation and intelligent micro-controller or bus-ASIC interface)
- 8-channel input according to IEC61131-2 (Type 1/2/3)
- Integrated galvanic isolation 500VAC (EN60664-1, UL1577)
- 3.3V/5V SPI and parallel micro-controller interface
- Adjustable deglitching filters
- Up to 500 kHz sampling frequency
- Wire-break detection
- VBB under-voltage detection
- Package: TSSOP-48, 8 mm x 12.5 mm

### Typical Application

Programmable Logic Controllers(PLC)

Industrial PC

General Control Equipment

### Description

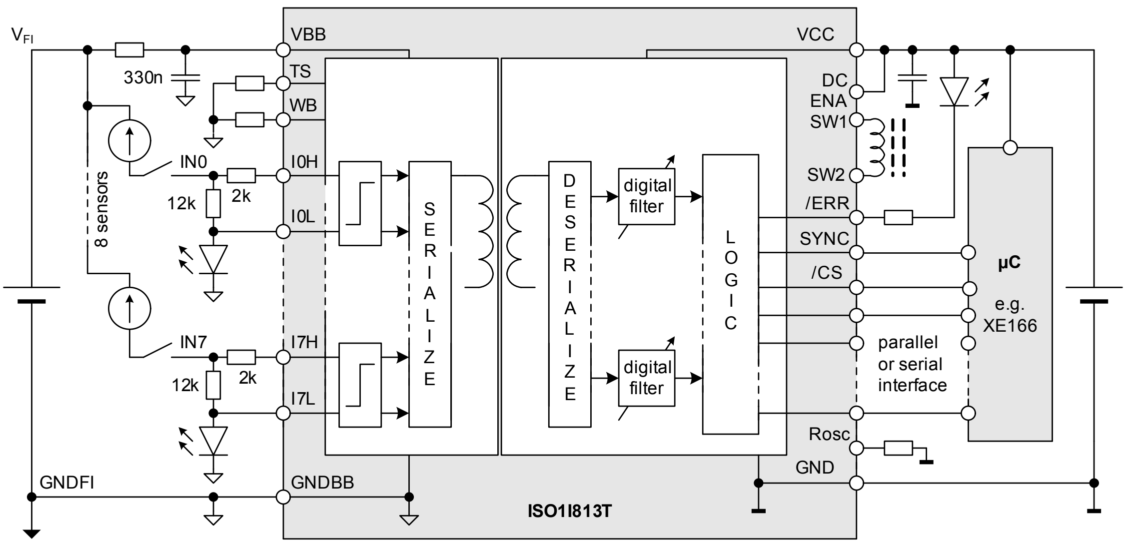
The ISO1I813T is an electrically isolated 8 bit data input interface in TSSOP-48 package.

This part is used to detect the signal states of eight independent input lines according to IEC61131-2 Type 1/2/3 (e.g. two-wire proximity switches) with a common ground (GNDFI).

For operating sensors of type 1/2/3 in accordance with IEC61131-2, it is necessary for the device to be wired with resistors $R_V$ and $R_{EXT}$ (it is recommended to use resistors with an accuracy of 2%, in any case < 5% - is mandatory, temperature-coefficients < 200ppm are allowed).

An 8 bit parallel µC compatible interface allows to connect the IC directly to a µC system. The input interface is designed to operate with 3.3/5V CMOS compatible levels.

The data transfer from input to output side is realized by the integrated Coreless Transformer Technology.




**Typical Application for Sensor of Type 1/3**

# 1 Pin Configuration and Functionality

The pin configuration slightly differs for the parallel or the serial interface.

## 1.1 Pin Configuration

The ordering, type and functions of the IC pins are listed in the **Table 1**.

**Table 1 Pin Configuration**

| Pin | Parallel Interface Mode | | | | Serial Interface Mode | | | |
|---|---|---|---|---|---|---|---|---|
| | Symbol | Ctrl 1) | Type 2) | Function | Symbol | Ctrl. 1) | Type 2) | Function |
| 1 | GND | | A | Logic Ground | GND | | | |
| 2 | SEL | I | PU | Serial Parallel Mode Select | SEL | | | |
| 3 | SYNC | I | PU | Freeze Data & Diagnostics | SYNC | | | |
| 4 | Rosc | | A | Clock Frequency Adjustment | Rosc | | | |
| 5 | VCC | | A | Positive 5/3.3V logic supply | VCC | | | |
| 6 | $\overline{ERR}$ | O | OD, PU | Fault Indication output | $\overline{ERR}$ | | | |
| 7 | GND | | A | Logic Ground | GND | | | |
| 8 | AD0 | IO | PPZ | Data output bit0 | SDI | I | PD | SPI Data input |
| 9 | AD1 | IO | PPZ | Data output bit1 | SSO | O | PPZ | SPI Status output |
| 10 | AD2 | IO | PPZ | Data output bit2 | GND | | | |
| 11 | AD3 | IO | PPZ | Data output bit3 | GND | | | |
| 12 | AD4 | IO | PPZ | Data output bit4 | $\overline{CRCERR}$ | O | OD, PU | CRC Error output |
| 13 | AD5 | IO | PPZ | Data output bit5 | SCLK | I | PD | SPI Shift Clock input |
| 14 | AD6 | IO | PPZ | Data output bit6 | SSI | I | PD | SPI Status input |
| 15 | AD7 | IO | PPZ | Data output bit7 | SDO | O | PPZ | SPI Data output |
| 16 | $\overline{CS}$ | I | PU | Chip Select | $\overline{CS}$ | | | |
| 17 | $\overline{RD}$ | I | PU | Data Read | n.c. | | | |
| 18 | GND | | A | Logic Ground | GND | | | |
| 19 | $\overline{WR}$ | I | PU | Data Write | MS0 | I | PD | SPI Mode Select bit 0 |
| 20 | ALE | I | PD | Address Latch Enable | MS1 | I | PD | SPI Mode Select bit 1 |
| 21 | DC_ENA | I | PD | DC-DC Supply Enable | DC_ENA | | | |
| 22 | SW1 | | A | DC-DC Switch Output 1 | SW1 | | | |
| 23 | SW2 | | A | DC-DC Switch Output 2 | SW2 | | | |
| 24 | GND | | A | Logic Ground | GND | | | |
| Sensor Side Pins | | | | | | | | |
| 25 | GNDBB | | A | Input Ground | GNDBB | | | |
| 26 | VBB | | A | Positive input supply voltage | VBB | | | |
| 27 | I0L | | A | Input 0 Low, LED Out | I0L | | | |
| 28 | I0H | | A | Input 0 High | I0H | | | |
| 29 | I1L | | A | Input 1 Low, LED Out | I1L | | | |
| 30 | I1H | | A | Input 1 High | I1H | | | |

Table 1 **Pin Configuration**

| Pin | Parallel Interface Mode | | | | Serial Interface Mode | | | |
|---|---|---|---|---|---|---|---|---|
| | Symbol | Ctrl 1) | Type 2) | Function | Symbol | Ctrl. 1) | Type 2) | Function |
| 31 | GNDBB | | A | Input Ground | GNDBB | | | |
| 32 | I2L | | A | Input 2 Low, LED Out | I2L | | | |
| 33 | I2H | | A | Input 2 High | I2H | | | |
| 34 | I3L | | A | Input 3 Low, LED Out | I3L | | | |
| 35 | I3H | | A | Input 3 High | I3H | | | |
| 36 | TS | | A | Sensor Type 1/2/3 Select | TS | | | |
| 37 | GNDBB | | A | Input Ground | GNDBB | | | |
| 38 | WB | | A | Wire Break Select | WB | | | |
| 39 | I4L | | A | Input 4 Low, LED Out | I4L | | | |
| 40 | I4H | | A | Input 4 High | I4H | | | |
| 41 | I5L | | A | Input 5 Low, LED Out | I5L | | | |
| 42 | I5H | | A | Input 5 High | I5H | | | |
| 43 | GNDBB | | A | Input Ground | GNDBB | | | |
| 44 | I6L | | A | Input 6 Low, LED Out | I6L | | | |
| 45 | I6H | | A | Input 6 High | I6H | | | |
| 46 | I7L | | A | Input 7 Low, LED Out | I7L | | | |
| 47 | I7H | | A | Input 7 High | I7H | | | |
| 48 | GNDBB | | A | Input Ground | GNDBB | | | |

1) Direction of the pin: I = input, O = output, IO = Input/Output

2) Type of the pin: A = analog, OD = Open-Drain, PU = internal Pull-Up resistor, PD = internal Pull-Down resistor, PPZ = Push-Pull pin with High-Impedance functionality

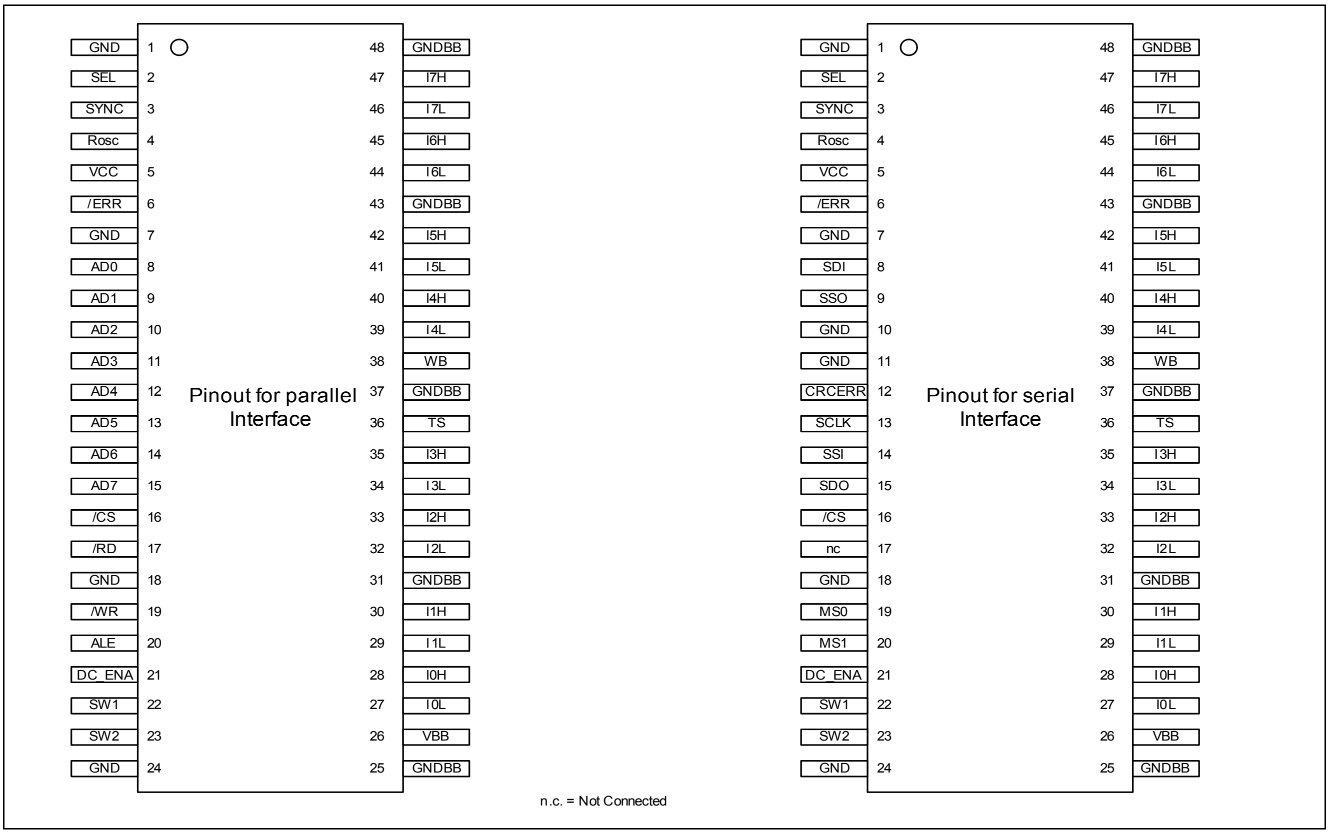



**Figure 1 TSSOP-48 Pinout for Parallel and Serial Interface Modes**

## 1.2 Pin Functionality

### 1.2.1 Pins of Sensor Interface

**VBB (Positive supply 9.6-35V sensor supply)**

VBB supplies the sensor input stage.

**GNDBB (Ground for VBB domain)**

This pin acts as the ground reference for the sensor input stage that is supplied by VBB.

**I0H... I7H (Input channel 0 ... 7)**

Sensor inputs with current sink characteristic according IEC61131-2 Type 1/2/3 which has been selected by pin TS

**I0L... I7L (LED output channel 0 ... 7)**

This pin provides the output signal to switch on the LED if the input voltage and current has been detected as "High" according to the selected type.

**WB (Wire-Break Select)**

By connecting a resistor between pin WB and pin GNDBB, the level for the Wire-Break detection can be adjusted (refer to **Table 10** for corresponding resistor value). This pin is for static configuration (pin-strapping). The input voltage at pin WB is not allowed to be changed during operation.

**TS (Type Select)**

By connecting a resistor between TS and GNDBB the sensor type (Type 1/2/3) can be selected (refer to **Table 10** for corresponding resistor value). This pin is for static configuration (pin-strapping). The input voltage at pin TS is not allowed to be changed during operation.

### 1.2.2 Pins of Serial and Parallel logic Interface

Some pins are common for both interface types, some others are specific for the parallel or serial access.

**VCC (Positive 3.3/5V logic supply)**

VCC supplies the output interface that is electrically isolated from the sensor input stage. The interface can be supplied with 3.3/5V.

**GND (Ground for VCC domain)**

This pin acts as the ground reference for the uC-interface that is supplied by pin VCC.

**Rosc (Clock Adjustment)**

A high precision resistor has to be connected between pin Rosc and pin GND to set the frequency of the sampling clock.

**DC_ENA (DC-DC Converter Enable)**

When the DC_ENA pin is connected to VCC, the internal DC-DC driver is activated. When DC_ENA is in the state Low, the switches are not driven. The input voltage must not change during operation. This pin has an internal Pull-Down resistor.

**SW1, SW2 (DC-DC switch outputs 1/2)**

When the pin DC_ENA is connected to VCC, the outputs SW1 and SW2 switch at the clock-frequency determined by the resistor at pin Rosc to supply the external push-pull converter. The switching frequency can be divided by two by setting the responsible bit in the GLCFG register (see also **Chapter 6**). Both outputs provide an open drain functionality.

**$\overline{\text{ERR}}$ (Error)**

The active Low $\overline{\text{ERR}}$ signal contains the OR-wired information of the sensor input undervoltage and missing voltage detection, the internal data transmission failure detection unit and the overcurrent fault of the DC-DC-converter. The output pin $\overline{\text{ERR}}$ provides an open drain functionality. During Start Up this pin $\overline{\text{ERR}}$ is pulled to High. This pin $\overline{\text{ERR}}$ has an internal Pull-Up resistor. In normal operation the signal $\overline{\text{ERR}}$ is High. See **Chapter 3.5** for more details.

**SEL (Serial or Parallel Mode Select)**

When this pin is in a logic Low state, the IC operates in Parallel Mode. For Serial Mode operation the pin has to be pulled into logic High state. During Start Up the IC is operating in Serial Mode. This pin has an internal Pull-Up resistor. This pin must not change during operation.

**SYNC**

When this pin is in a logic High state, the IC operates in continuous mode with the internal sampling clock. In isochronous mode, the internal data and diagnostics registers are synchronized on each falling edge detected at SYNC. The internal data and diagnostics registers are frozen with the falling edge of SYNC. In logic Low state the internal data and diagnostic registers are not updated. During Start-Up this pin is pulled to High state. This pin has an internal Pull-Up resistor. (see also **Chapter 3.9**)

**$\overline{\text{CS}}$ (Chip Select)**

When the pin $\overline{\text{CS}}$ pin is logic Low, the IC interface is enabled and data can be transferred. This pin $\overline{\text{CS}}$ has an internal Pull-Up resistor.

**The following pins are provided in the parallel interface mode**

**AD7:AD0 (AddressData input / output bit7 ... bit0)**

The pins AD0 .. AD7 are the bidirectional input / outputs for data write and read. Depending on the state of the pins ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$ and the AD7 bit register addresses or data can be transferred between the internal registers and the parallel interface of a e.g. micro-controller .

**$\overline{\text{RD}}$, $\overline{\text{WR}}$ (Read / Write)**

By pulling one of these pins down, a read or write transaction is initiated on the AddressData bus and the data becomes valid. These pins have internal Pull-Up resistors.

**ALE (Address Latch Enable)**

The pin ALE is used to select between address (ALE is in a logic High state) or data (ALE is in a logic Low state). Furthermore, a read or write transaction can be selected in conjunction with the AD7 bit. When ALE is pulled high, addresses are transferred and latched over the bit AD0 to AD6. The AD7 bit serves for a read access (AD7 is Low) or a write access (AD7 is High) at this address. During the Low State of ALE all transactions hit the same adress. This pin has an internal Pull-Down resistor.

**The following pins are provided in the serial interface mode**

**MS0, MS1 (Serial Mode Select)**

By driving the pins MS, MS1 to Logic High or Logic Low the Serial Interface Mode can be selected. These pins have internal Pull-Down resistors. The mode of the Serial Interface can be changed by the user during operation.

**SCLK (Serial interface shift clock)**

Input data are sampled with the rising edge and output data are updated with the falling edge of this input clock signal. This pin SCLK has an internal Pull-Down resistor.

**SDI, SSI (Serial interface data/status input )**

SDI/SSI data is put into a dedicated FIFO to program the filtering time and mask the Wire-Break diagnostic bits of each channel (SPI Mode 2 and 3). It is also used to set the address of the register, which is intended to be accessed. This pin has an internal Pull-Down resistor.

**SDO, SSO (Serial interface data/status outputs)**

SDO provides the sensor data bits and or the register content, SSO provides the sensor diagnostics bits.

**$\overline{\text{CRCERR}}$ (CRC Error output)**

This pin $\overline{\text{CRCERR}}$ is in a logic Low state when CRC errors or Shift-Clock errors are detected internally. This pin $\overline{\text{CRCERR}}$ provides an open drain functionality. This pin has an internal Pull-Up resistor.

# 2 Blockdiagram

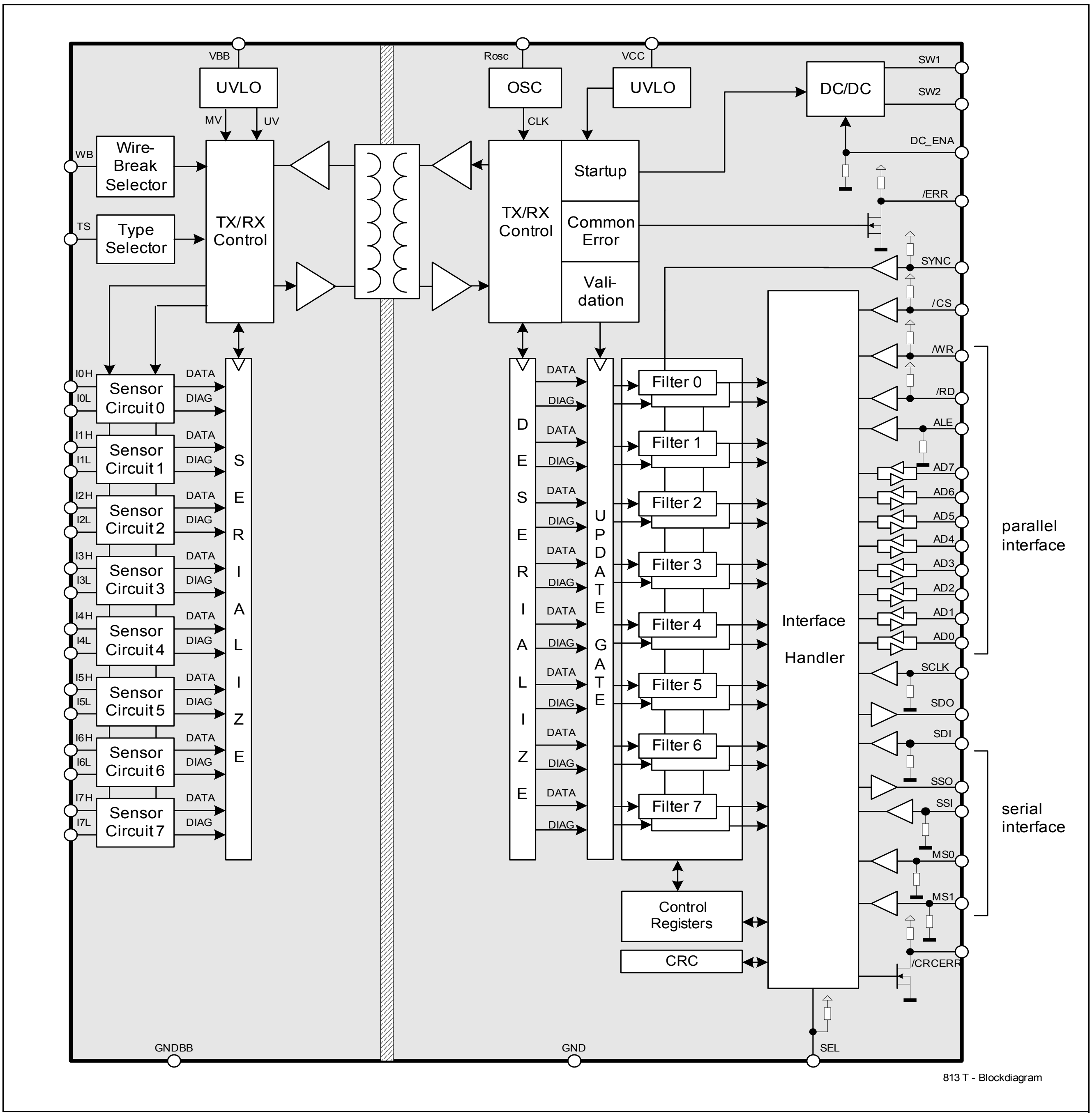



**Figure 2 Block Diagram ISO1I813T**

# 3 Functional Description

The ISO1I813T is an electrically isolated 8 bit data input interface. This part is used to detect the signal states of eight independent input lines according to IEC61131-2 Type 1/2/3 (e.g. two-wire proximity switches) with a common ground (GNDBB).

## 3.1 Introduction

The current in the input circuit is determined by the switching element in state “0” and by the characteristics of the input stage in state “1”.

The octal input device is intended for a configuration comprising two specified external resistors per channel, as shown in **Figure 10 “Typical Application for Sensor Input Type 1, 2 and 3” on Page 19**. As a result the power dissipation within the package is at a minimum.

The voltage dependent current through the external resistor $R_{EXT}$ is compensated by a negative differential resistance of the current sink across pins IxH and IxL, therefore input INx behaves like a constant current sink.

The comparator assigns level 1 or 0 to the voltage present at input IxH. To improve interference protection, the comparator is provided with hysteresis. A status LED is connected in series with the input circuit ($R_{EXT}$ and current sink).

If no LED is used an external resistor of 2 kΩ (type 1 and 3) has to be connected between IxL and GNDBB. The specified switching thresholds may change if the LED is replaced by a resistor.

The internal LED drive short-circuits the status LED if the comparator detects “0”. A constant current sink in parallel with the LED reduces the operating current of the LED, and a voltage limiter ensures that the input circuit remains operational if the LED opens, but the switching thresholds may change.

For each channel an adjustable digital filter is provided which samples the comparator signal at a rate configured by programming internal registers. The digital filter is designed to provide averaging characteristics. If the input value remains the same for the selected number of sampling values, then the output changes to the corresponding state.

The µC compatible interfaces allow a direct connection to the ports of a microcontroller without the need for other components. The diagnostic logic on the chip monitors the internal data transfer as well as the sensor input supply. The information is sent via the internal coreless transformer to the pin $\overline{ERR}$ at the input interface

## 3.2 Power Supply

The IC contains two electrically isolated voltage domains that are independent from each other. The microcontroller interface is supplied via pin VCC, GND and the input stage is supplied via pin VBB, GNDBB. The different voltage domains can be switched on at different times. **Figure 4** shows the Start Up behaviour if both voltage domains are powered by an external power supply. If the VCC and VBB voltage have reached their operating range and the internal data transmission has been started successfully, the IC indicates the end of the Start Up procedure by setting the pin $\overline{ERR}$ to logic low. In the situation of a supply voltage drop at VBB on the Sense Side - even short - the Sense Chip requires a proper restart and therefore the µController Side control unit needs to react accordingly, especially to guarantee the integrity of the sensor data provided to the filter stage.

### 3.2.1 Voltage Limits on VBB

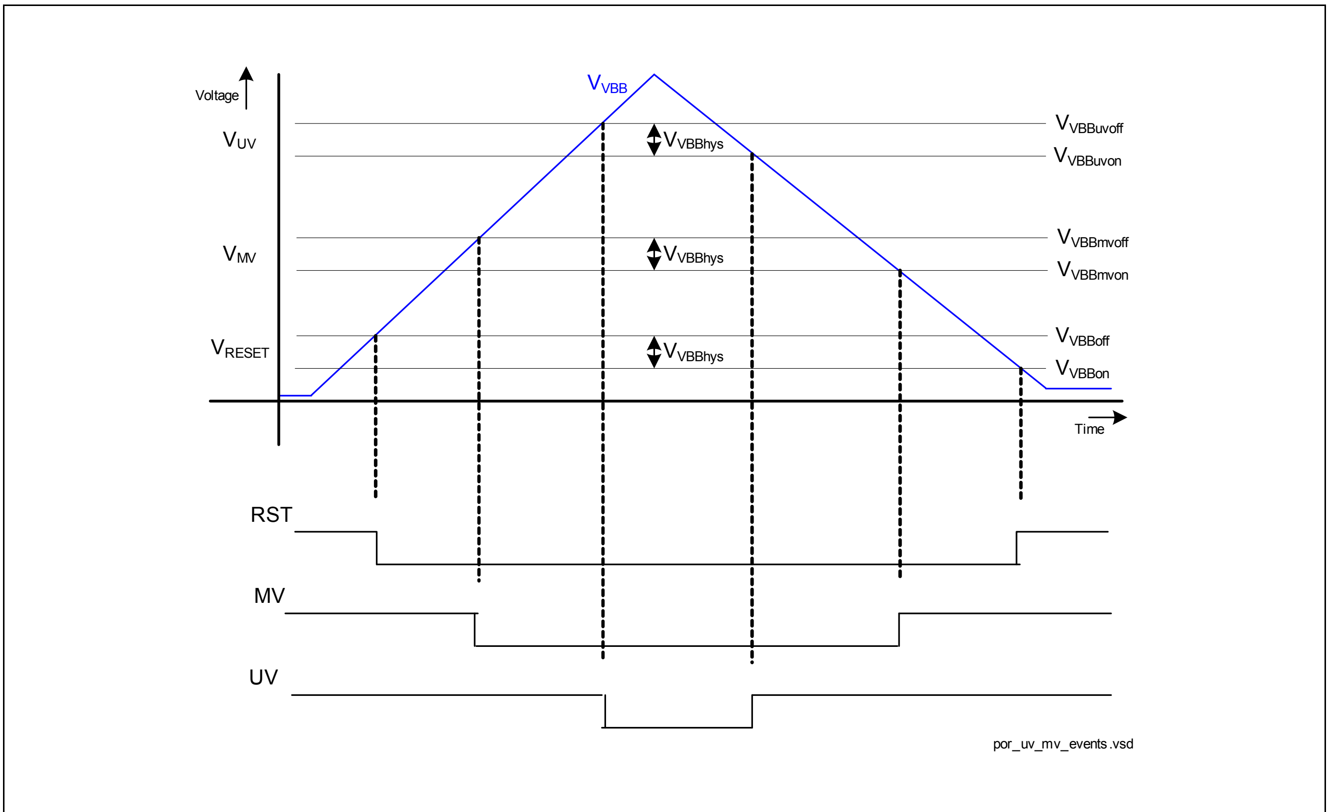



**Figure 3 Start Up Procedure with external Power Supply**

During UVLO, all registers are reset to their reset values as specified in the **Chapter 6.2**. As a result, the flags TE, UV as well as MV are High and the ERR pin is Low (error condition). Immediately after the reset is released, the IC is first configured by "reading" the logic level of the SEL, MS1, MS0 (when available). The IC powers up as a serial device (SEL has a pull-up resistor).

The supply voltage VBB is monitored during operation by two internal comparators (with typ. 8 µs blanking time @ 500kHz $f_{scantyp}$) detecting:

- VBB Undervoltage: If the voltage drops below the UV threshold (see **Table 7**), the UV-bit in the **GLERR** register is set High. The IC remains in normal operation.
- VBB Missing Voltage: If the voltage further drops below the MV threshold, lower than the previous threshold, the MV-bit in the **GLERR** register is set, the Sense Side of the IC is turned off when reaching the $V_{RESET}$ threshold whereas the Micro-Controller Side remains active.

These 2 thresholds are inactive when the IC operates in Self Power Mode i.e. when the DC_ENA pin is High.

*Note: In case DC_ENA is High the integrated DC/DC driver is active. The driver stage is self-protected in overload condition: the internal switches will be turned off as long as the overcurrent condition is detected and the IC will automatically restart once the overload condition disappears.*

**Important:** Since the UV and MV (as well as the TE and W4S) bits used for generating the ERR signal are preset to High during UVLO, the ERR pin is Low after power up. Therefore the ERR signal requires to be explicitly cleared after power up. At least one read access to the GLERR and INTERR registers is needed to update those status bits and thus release the ERR pin.

### 3.2.2 External Supply

Figure 4 shows the Start Up behaviour if both voltage domains are powered by an external power supply. If the VCC and VBB voltage have reached their operating range and the internal data transmission has been started successfully, the IC indicates the end of the Start Up procedure by setting the pin ERR to logic low.

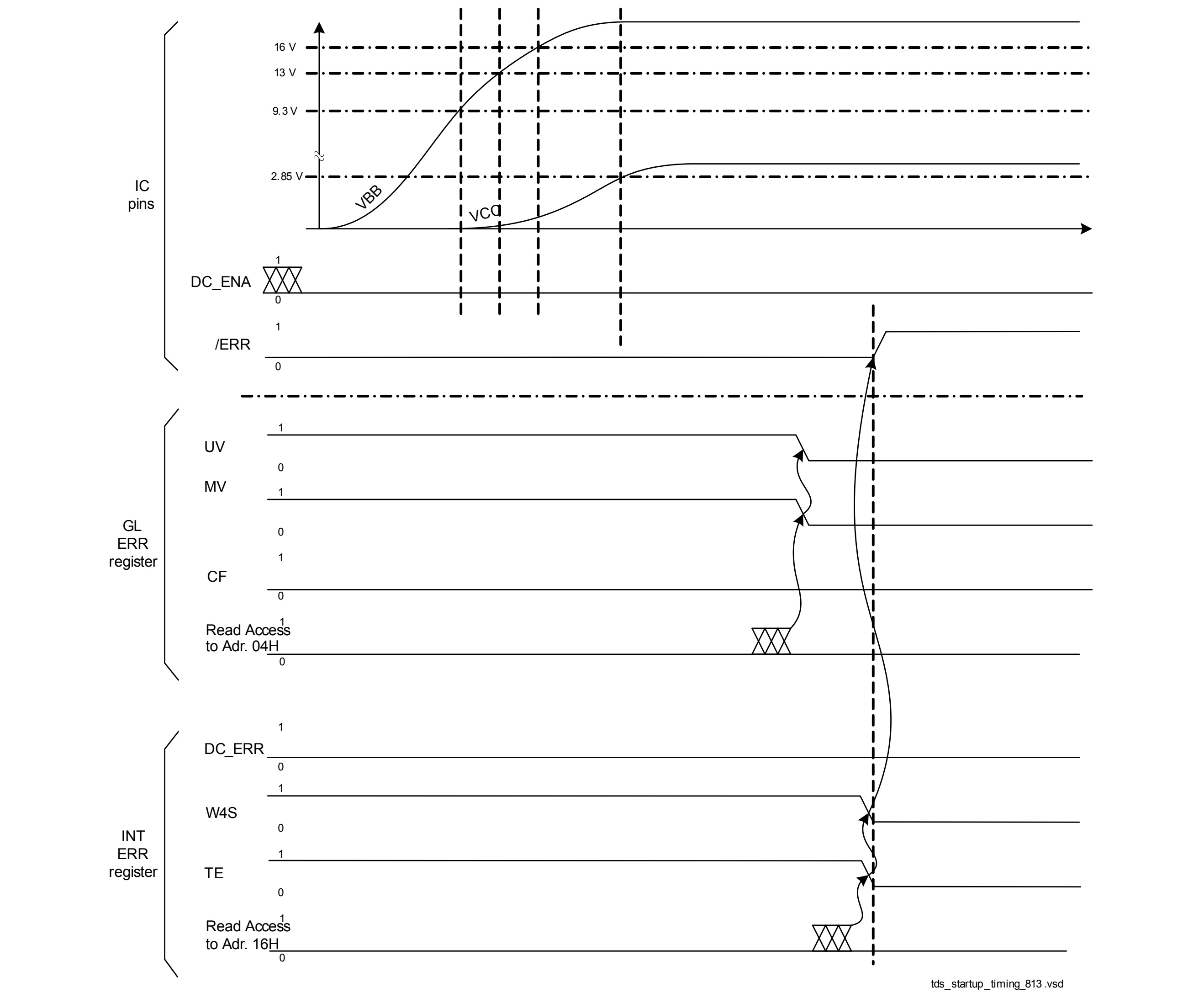



**Figure 4 Start Up procedure with external power supply**

### 3.2.3 DC/DC Supply

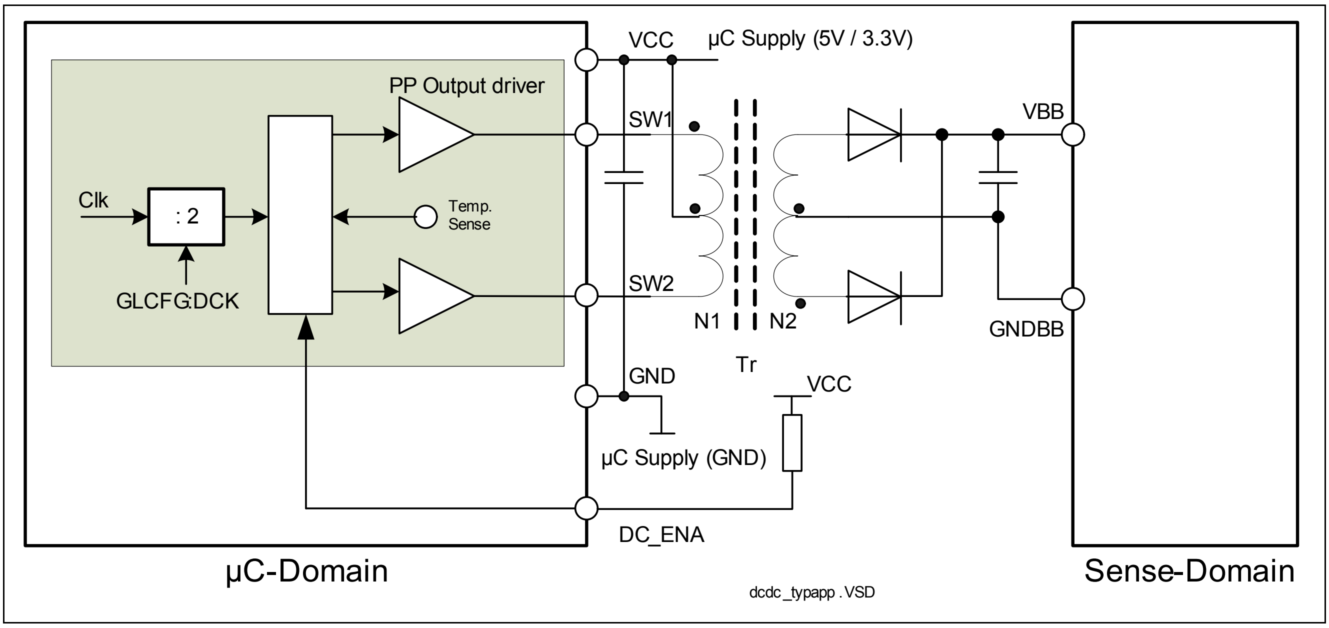



**Figure 5 Typical Circuitry for Self Powered Mode with Push-Pull Converter**

The IC can as well operate in self powered mode. In this case, the Process Side (Sense-Domain) can be supplied at VBB with an isolated push-pull converter connected to the Micro-controller Side and driven by the pins SW1 and SW2 . The internal driver stage at SW1 and SW2 is designed to power up two ISO1I813T (refer to **Table 8**). The DC/DC-Converter is driven by the internal clock. Parameters are calculated with the internal clock of 500 kHz. By setting the DCK Bit in the GLCFG register a prescaler by 2 can be activated. Should the user adjust the internal clock to a different frequency the transformer has to be adjusted accordingly.

The short-circuit protection uses a temperature sensor located close to the drivers and disables the driver stages when a predefined temperature is reached (**Figure 7**, **Figure 5**). The target value for the switch-off-temperature is 160°C with a hysteresis of < 10°C. That means that the drivers are switched off at a junction temperature of 160 °C and switched on at a junction temperature of <=150°C

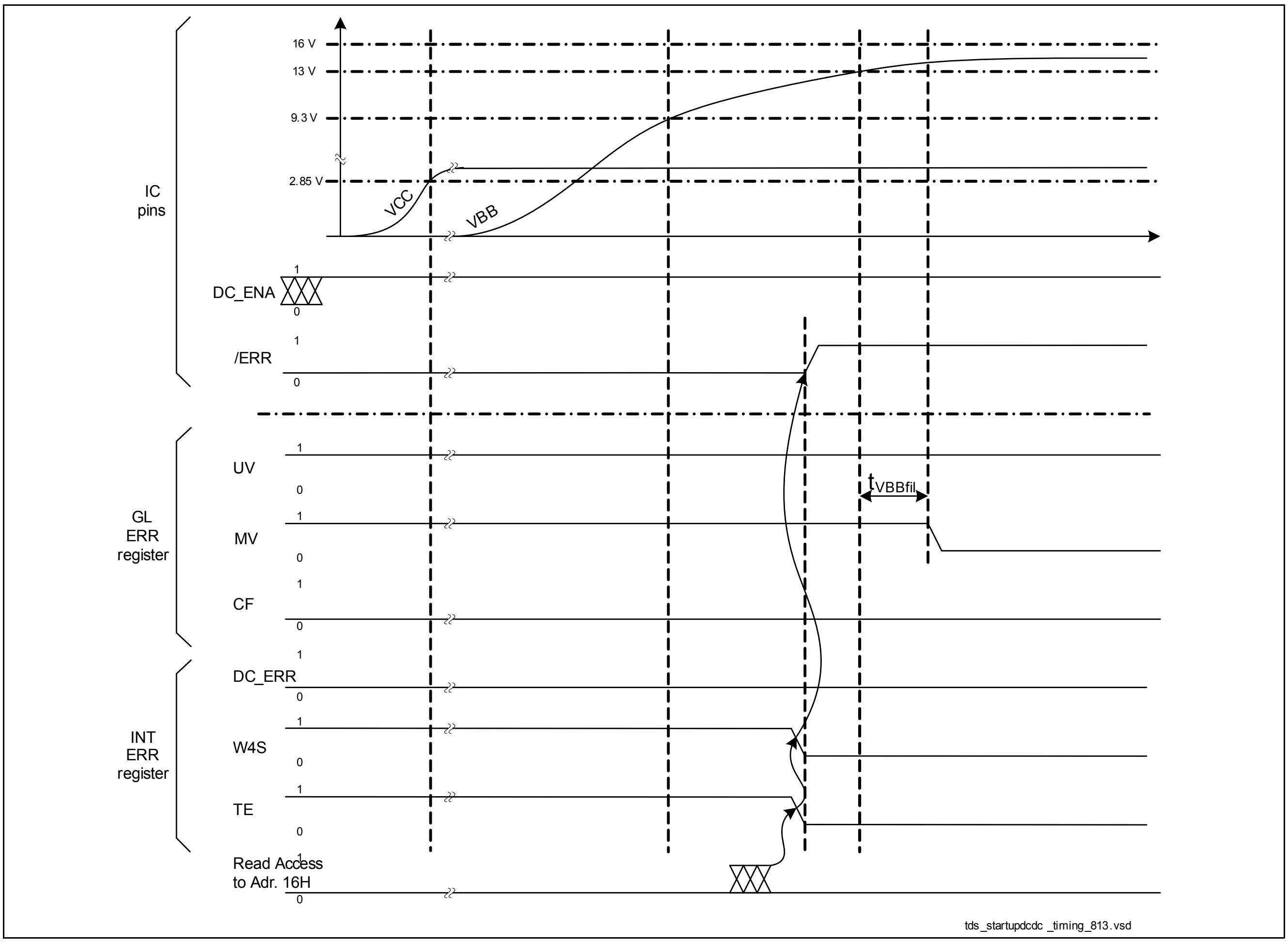



**Figure 6 Start Up Procedure with DC/DC Supply**

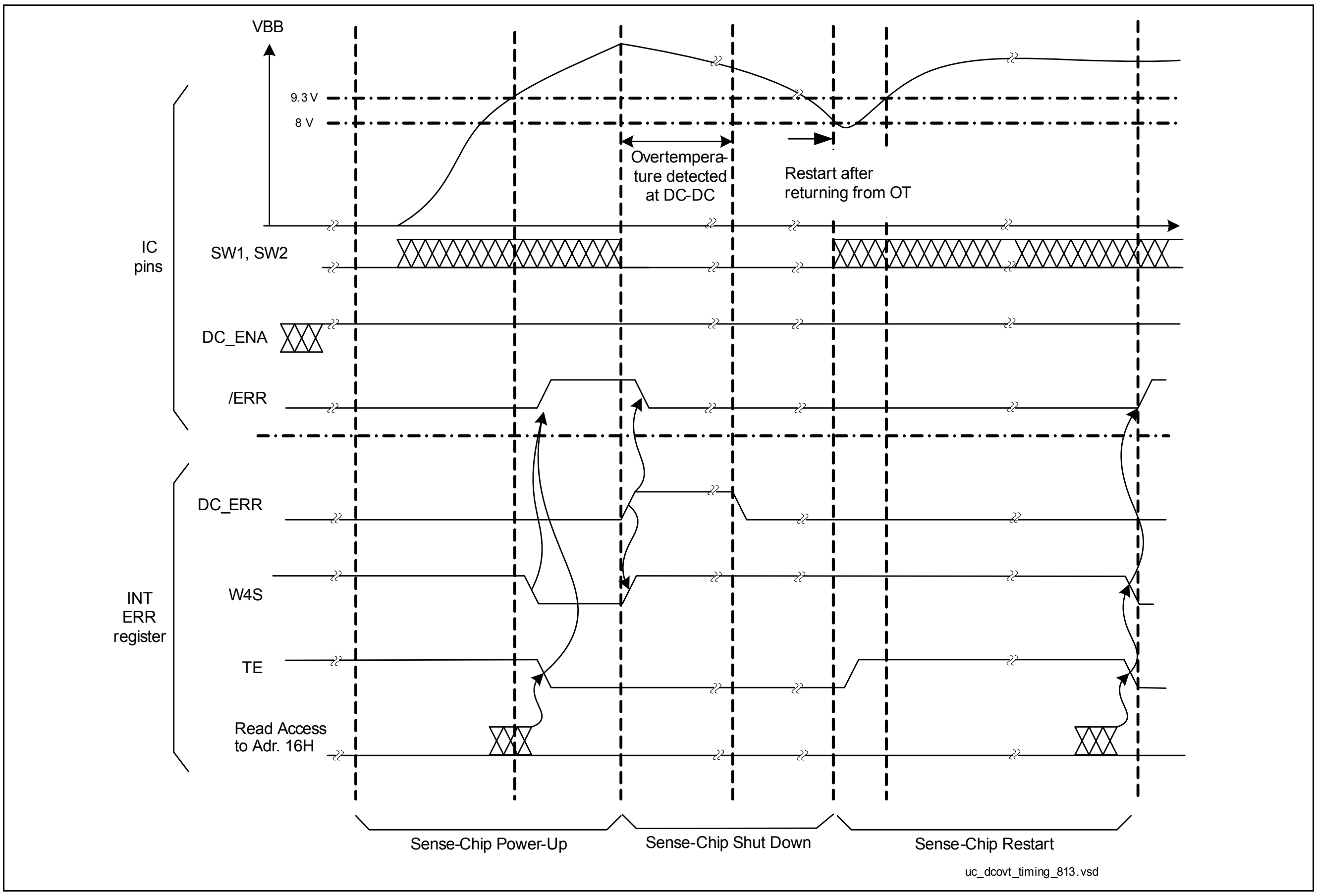



**Figure 7 Restart Procedure after VBB drop due to DC/DC Supply Overtemperature**

## 3.3 Internal Oscillator

An external resistor has to be connected to Rosc and allows the adjustment of the frequency as shown in **Figure 8**.

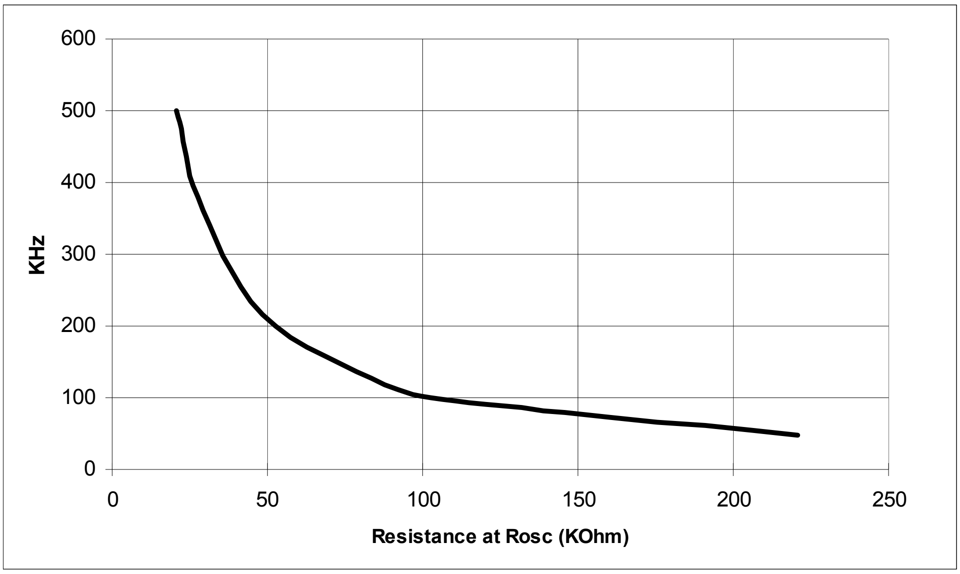



**Figure 8 Internal Frequency Setting at Rosc**

The internal oscillator provides the scan clock for the sampling of the sensor data and diagnostics as well as for the internal digital averaging filters. Therefore the filter times as defined in the **Table 11** for the typical frequency of 500 KHz will change accordingly. As an example, it is possible to define filter time longer than 20 ms by reducing the internal oscillator frequency.

Moreover, in the applications where the IC current consumption is critical, it is possible to reduce the internal oscillator frequency by increasing the $R_{OSC}$ (see **Figure 9**).

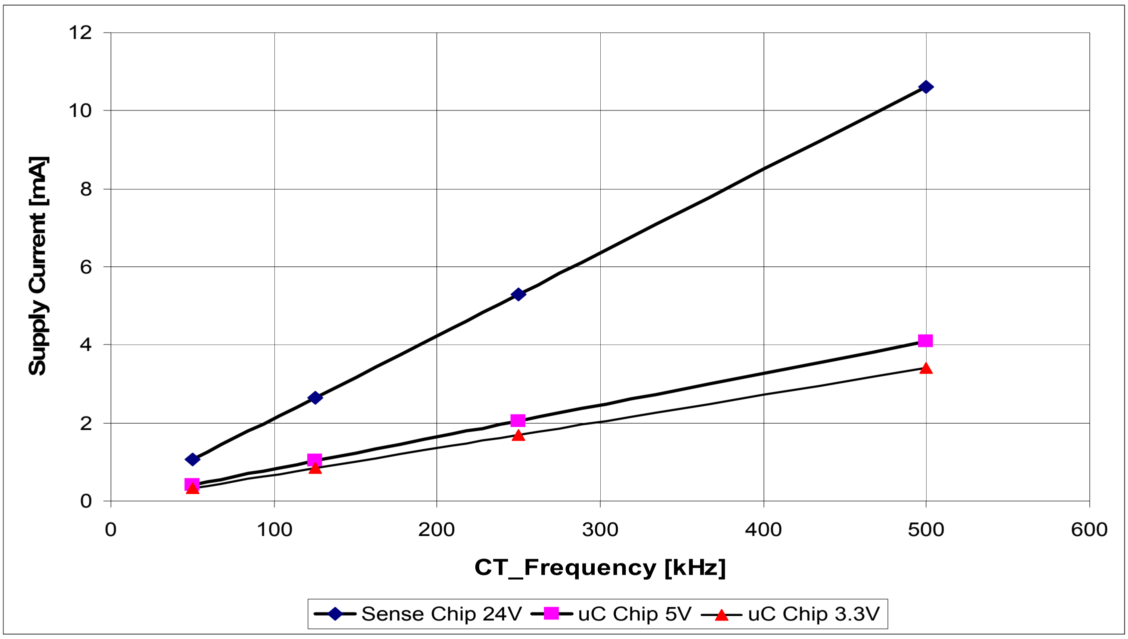
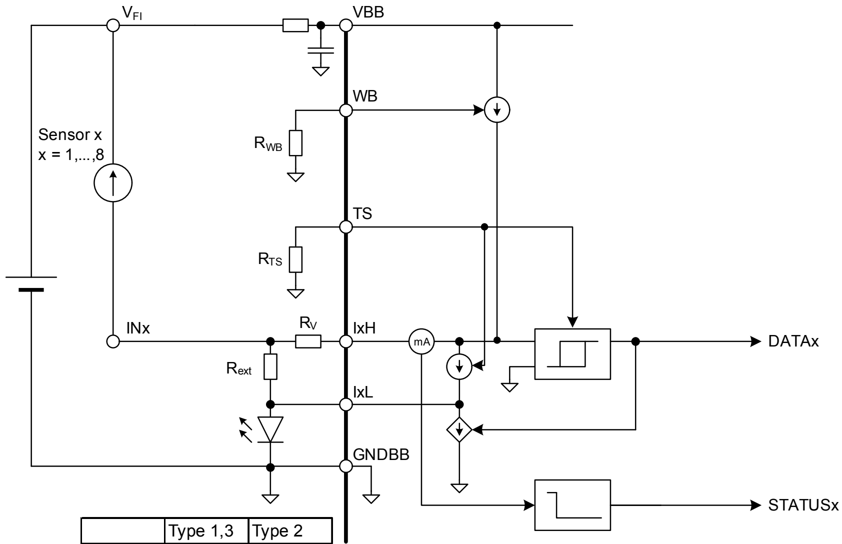



**Figure 9 IC Current Consumption in function of the internal frequency**

## 3.4 Sensor Input

### 3.4.1 Input Type Select

The sensor input structures are shown in **Figure 10** (Type 1,2,3). Due to its active current a V-I-characteristic as shown in **Figure 11** is maintained. This V-I-curve is well within the IEC 61131 standard requirements of Type 1, Type 2 and Type 3 sensors, respectively. The **Figure 12** shows the typical application for sensor of type 2. It is recommended to choose for the external resistors $R_{EXT}$, $R_V$, $R_{LED}$ an accuracy of 2 % (< 5% is mandatory) otherwise the V/I-characteristic shown in **Figure 11** cannot be guaranteed.




| | Type 1,3 | Type 2 |
|---|---|---|
| $R_V$ | 2kΩ | 1.5kΩ |
| $R_{ext}$ | 12kΩ | 8.5kΩ |

**Figure 10 Typical Application for Sensor Input Type 1, 2 and 3**

The filtered input-data information is visible in the Input Channel Data Register : **INPDATA** and is also described by the nomenclature : input-data.

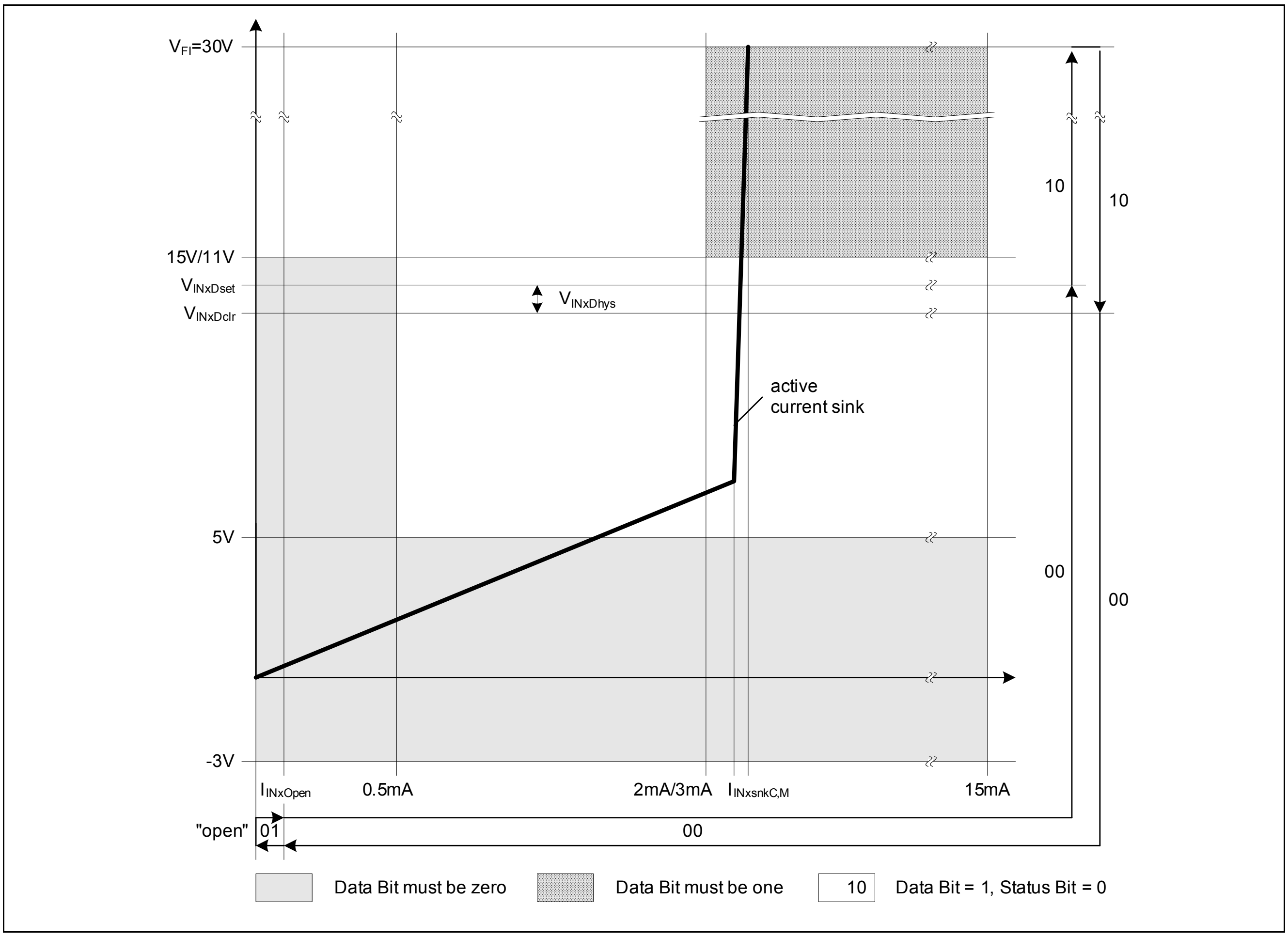



**Figure 11 Sensor Input Characteristics**

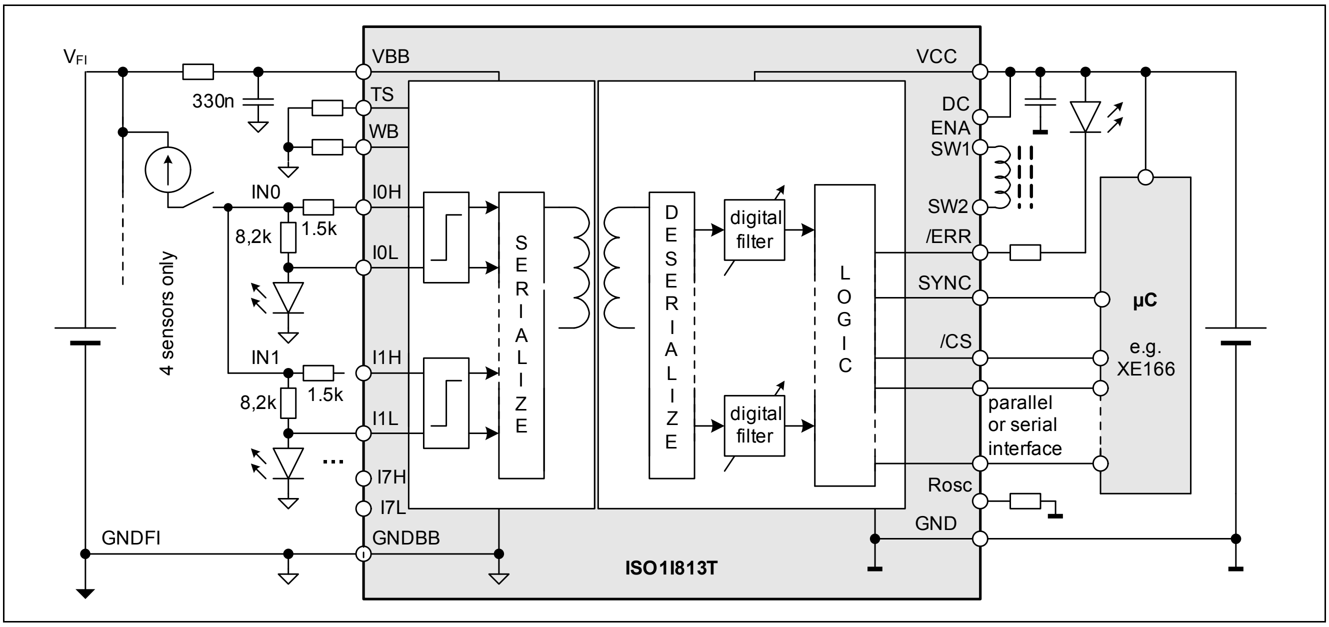



**Figure 12 Typical Application for Sensor Type 2**

### 3.4.2 Wire Break Detection

The wire-break current can be adjusted by the $R_{WB}$-resistor value connected to the pin WB (Figure 13). The minimum wirebreak-current can be choosen only when a LED- or Zener-Diode is connected to the pin IxL with a forward current in the range of few uA in the voltage range below 1 V. In the case of a connected resistor at IxL a large current is flowing across the external resistor Rext and the IxL-resistor ($R_{LED}$). This part cannot be measured internally and has to be added to the internal current part. In this case the minimum adjustable current is 230uA ($R_{LED}$ = 2kOhm). The WB bits in the status register have a sticky (latched) property and remains set as long as they are not cleared by a read access and the fault condition is not detected anymore.

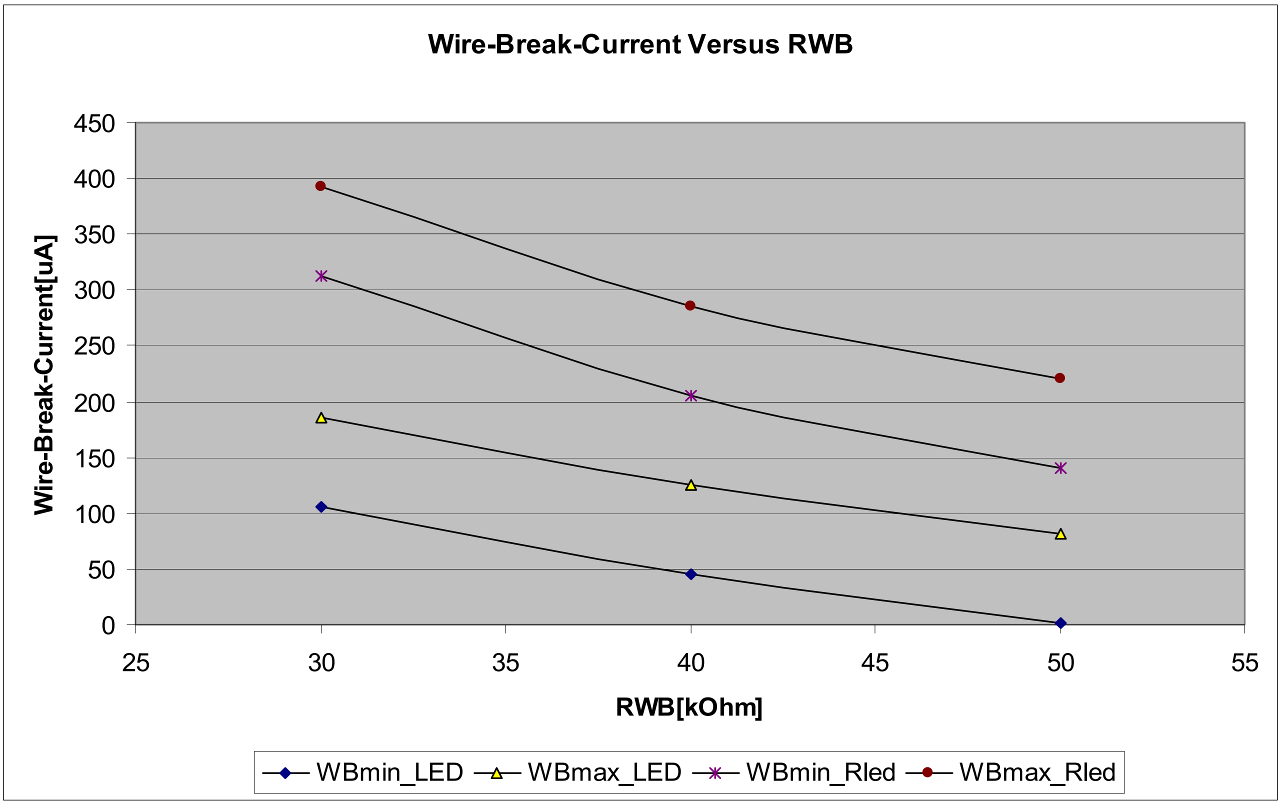



**Figure 13 Wire Break Detection for Type 1,3 (typ. @ 25°C)**

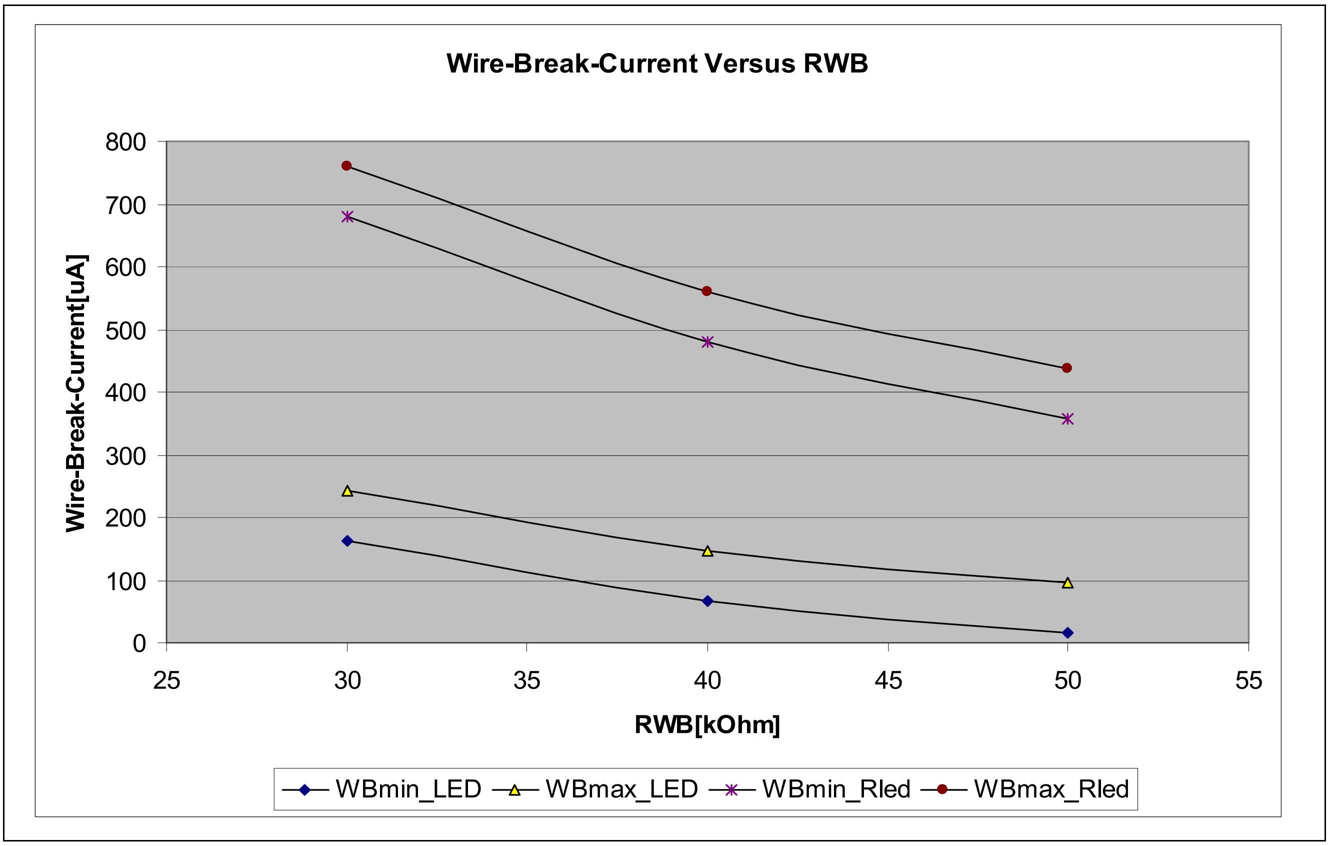



**Figure 14 Wire Break Detection for Type 2 (typ. @ 25°C)**

In the case of Type 2 two sense inputs are switched in parallel to achieve 2 * 3 mA (**Figure 12**). In each sense input a mimimum wirebreak current of 60 µA can be measured which means in sum a minimum wirebreak current of 120 µA. It is not recommended to use external resistors at the pins IxL in case of wirebreak measurements. The recommended value would be $R_{LED}$ = 1.2 kΩ which has been choosen in order not to produce a large voltage drop between IxL and GNDBB which in turn would limit the voltage drop across the sink. The low value of $R_{LED}$ would cause a high external current in case of wirebreak-measurements which has to be multiplied by two due to the parallel circuitry of the sense inputs.

The filtered wirebreak-diagnosis is visible in the Collective Diagnostic Register : **DIAG** and is also described by the nomenclature: status.

## 3.5 Common Error Output

The input (VBB) undervoltage and missing voltage status which are transmitted via the integrated coreless transformer to the output block and the internal data transmission monitoring information are evaluated in the common error output block, see **Figure 15**. In self-powered mode, extra information in case of over-current at SW1/2 is evaluated as well.

In case of an internal data transmission error the data and status bits are replaced by the last valid transmission. Moreover, if four consecutive erroneous data transmissions (TE1=1) occur, an internal error signal (TE4=1) is set. The averaging filters are reset and this status is held until four consecutive error-free transmissions (TE1=0) occur. An example timing diagram is shown in **Figure 15**.

This internal error signal is OR-wired with the current VBB undervoltage and missing voltage status. Additionally in the ISO1I813T, the Collective Diagnostics flag is combined in the $\overline{\text{ERR}}$. Since the output error signal is active-Low, the OR-wired result is negated.

In the Self Powered mode, the UV and MV are masked out. Instead the DC_ERR bit of the register **INTERR** is combined with the Transmission Error signal and output at the pin ERR.

The output stage at pin ERR has an open drain functionality with a pull-up resistor. See **Table 13** for the electrical characteristics.

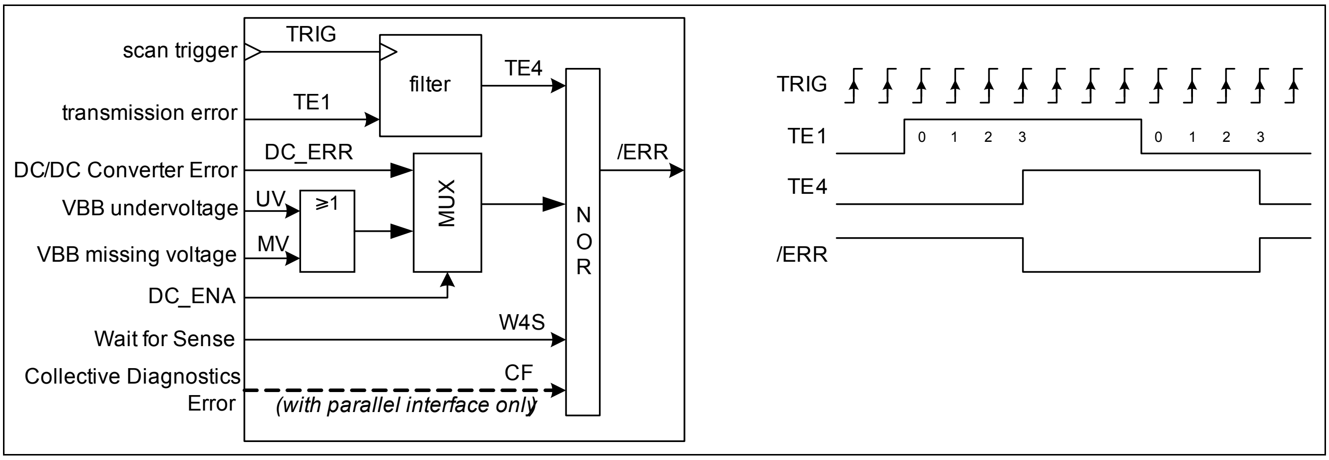



**Figure 15 Common Error Output**

## 3.6 Programmable Digital Input Filter

The sensor data and diagnosis bits of each input channel can be filtered by a configurable digital input filter. If selected, the filter changes its output according to an averaging rule with a selectable average length. When the sensor state changes without any spikes and noise the change is delayed by the averaging length. Sensor spikes that are shorter than the averaging length are suppressed. Figure 16 shows the behaviour of the filter. The clock of the Digital Filter is supplied from the internal oscillator. Therefore the filtertime depends on the oscillator frequency setting. For the filtering times of 1.6 msec , 3.2 msec , 10 msec , 20 msec a prescaler was used. Therefore the update interval was choosen to be 4 usec, 8 usec, 64 usec , 64 usec respectively (based on 500 kHz clock).

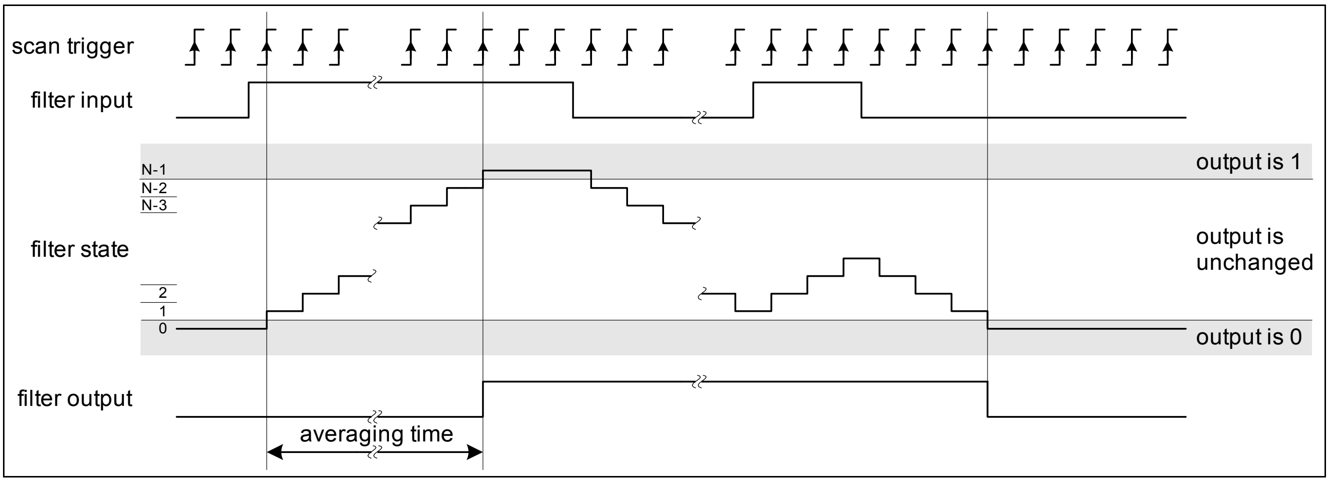



**Figure 16 Digital Filter Behavior**

The averaging length is selected for each channel individually using the configuration registers COEFIL0-7. The programmed filter time apply for both the data and the diagnostics of one channel. See Table 11 for the different setting options including filter bypass.

Figure 17 and Table 17 describe the timing for changing filter-coefficients. Especially timing restrictions have to be obeyed implying a minimal processing time until the new configuration and the filtered data are valid and can e.g. be frozen with the pin SYNC. Changing the filter coefficients means resetting always the related filter.

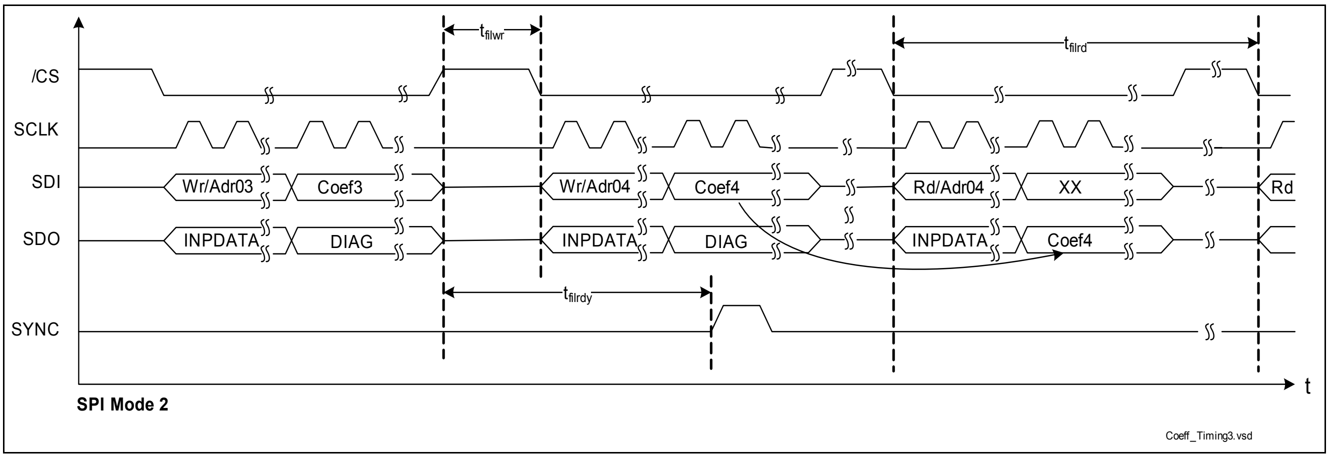



**Figure 17 Filter Time Programming and Update Timing**

Whereas the absolute filter time depends on the internal oscillator frequency accuracy, the maximal jitter per channel of the IC is 1.5 %. The channel jitter defined in the Figure 18 is due to the sampling error of the sensor data with the internal clock and applies equally for all the channels.

Furthermore, a fixed propagation delay has to be taken into account due to the data transmission over the Coreless Transformer.

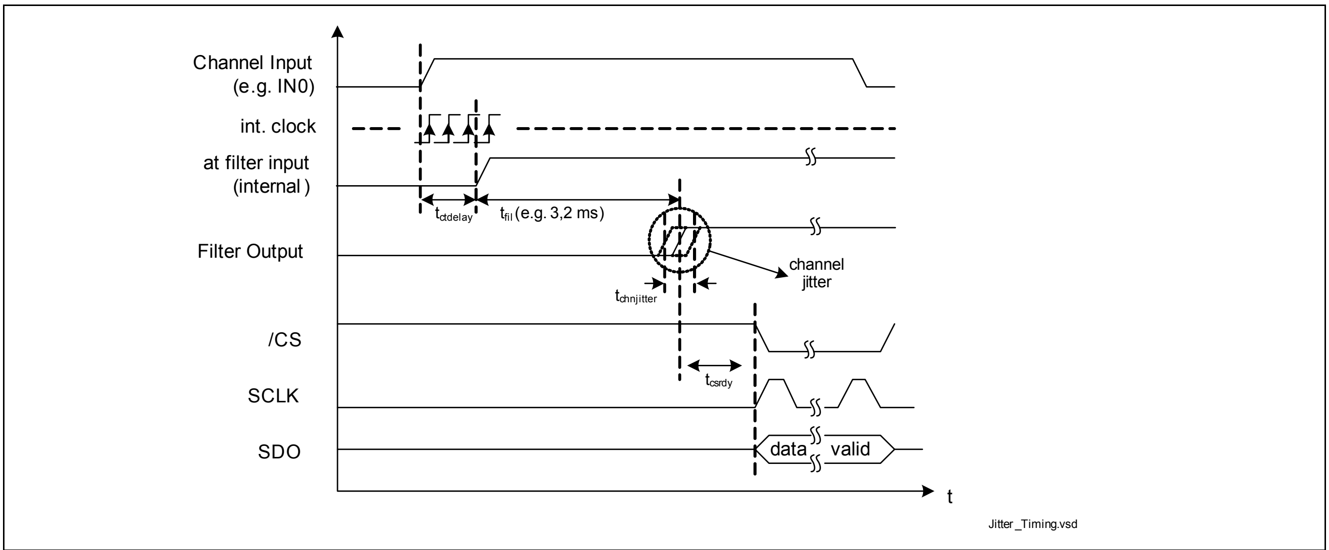



**Figure 18 Channel Jitter Definition**

## 3.7 Parallel Interface Mode

The ISO1I813T contains a parallel interface that can be selected by pulling the pin SEL to logic Low state. The interface can be directly controlled by the microcontroller output ports. (**Figure 19**). The output pins AD7:AD0 are in state "Z" as long as $\overline{\text{CS}}$=1. Otherwise, new sensor data bits (Input-Value) or diagnosis bits (Status) are driven with the falling edge of $\overline{\text{RD}}$ and provided at pins AD7:AD0. Incoming data for a write access are sampled with the rising edge of $\overline{\text{WR}}$.

Although write- and read-commands can be distinguished by the pins $\overline{\text{WR}}$ and $\overline{\text{RD}}$ additionally the MSB of the address-byte has to be set or not set (analog to the serial access). Write commands are configured with the MSB of the addess-byte set to "1", read commands are configured with the MSB of the address-byte set to "0".

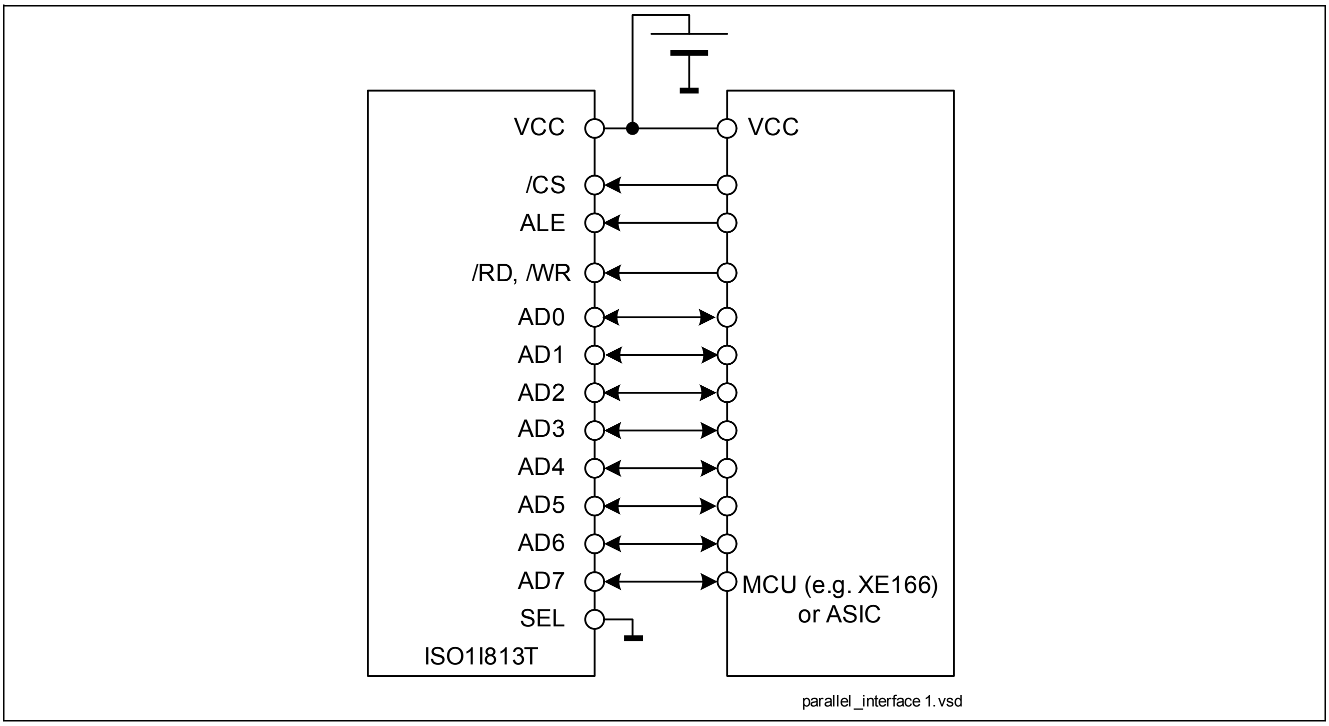



**Figure 19 Bus Configuration for Parallel Mode**

The timing requirements for the parallel interface are shown in **Figure 20**, **Figure 21** and **Table 15**.

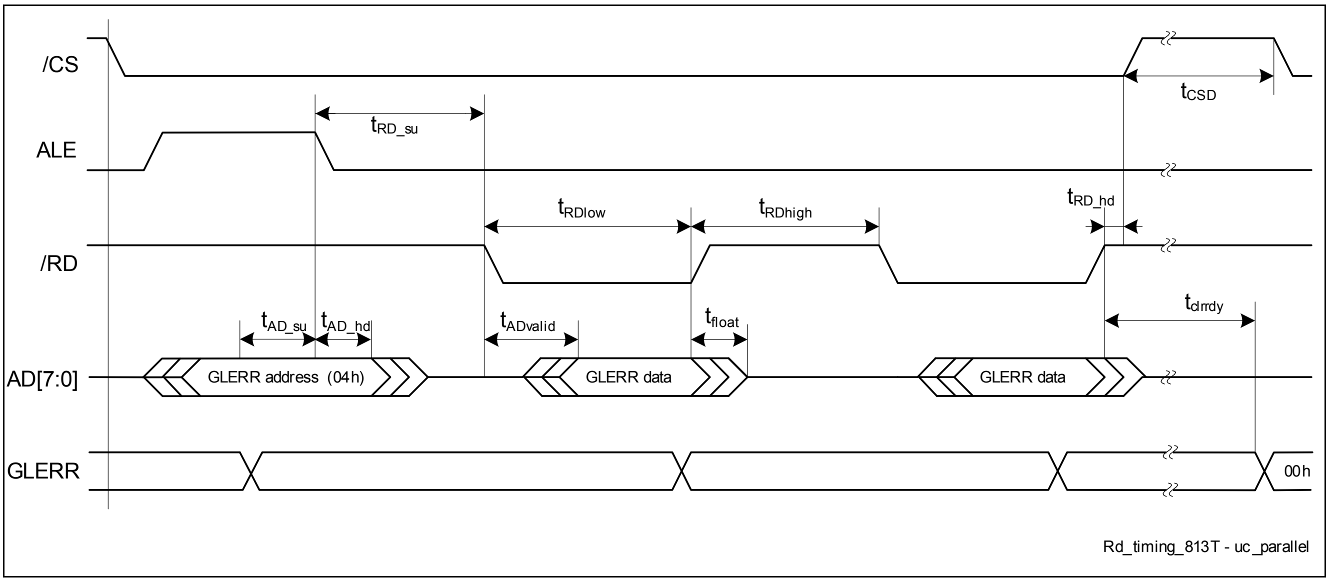



**Figure 20 Parallel Bus Timing Read**

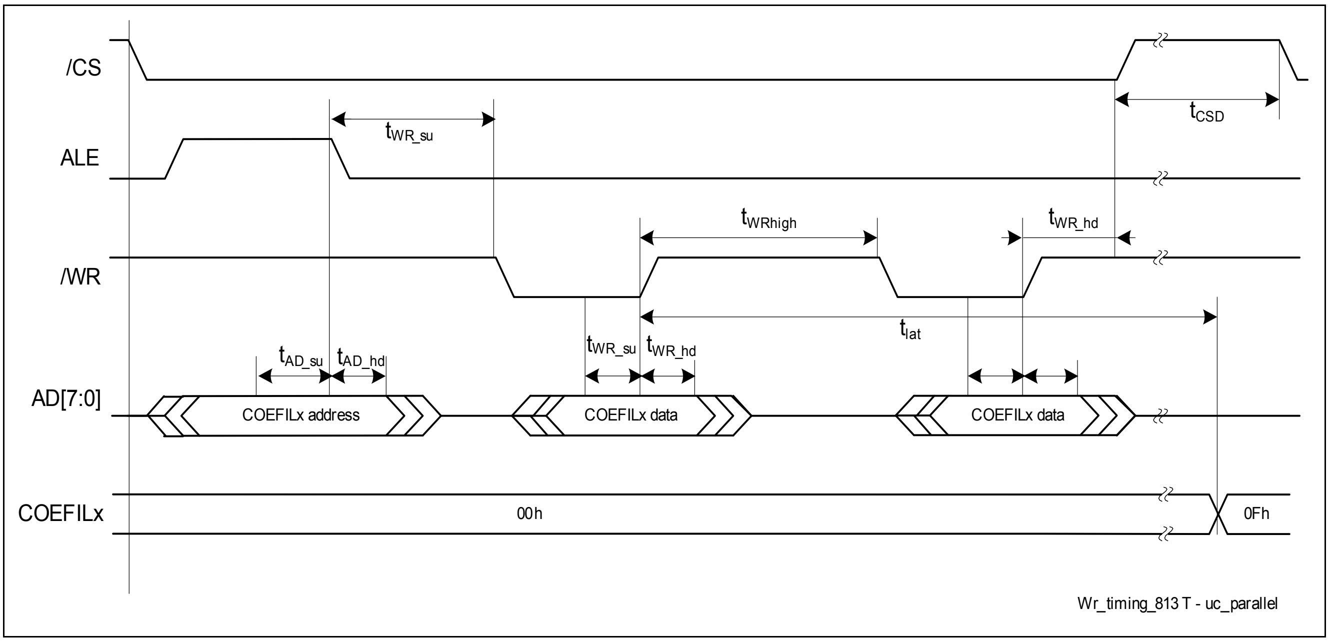



**Figure 21 Parallel Bus Timing Write**

## 3.8 Serial Interface Mode

The ISO1I813T contains two serial interfaces that can be activated by pulling the pin SEL to logic High state. The interface can be directly controlled by the microcontroller output ports. The output pins SDO and SSO are in state "Z" as long as $\overline{CS}$=1. Otherwise, the bits are sampled with the falling edge of $\overline{CS}$. With every falling edge of SCLK the bits are provided serially to the pin SDO and SSO respectively. At the same time, the inputs to SDI, SSI are registered into input-FIFO buffers (sampled with the rising edge of SCLK). When all internally sampled bits have been transferred to SDO/SSO, the buffered bits from the inputs SDI/SSI are provided to these pins (daisy-chain support).

The timing requirements for the serial interface are shown in **Figure 22** and in **Table 16**.

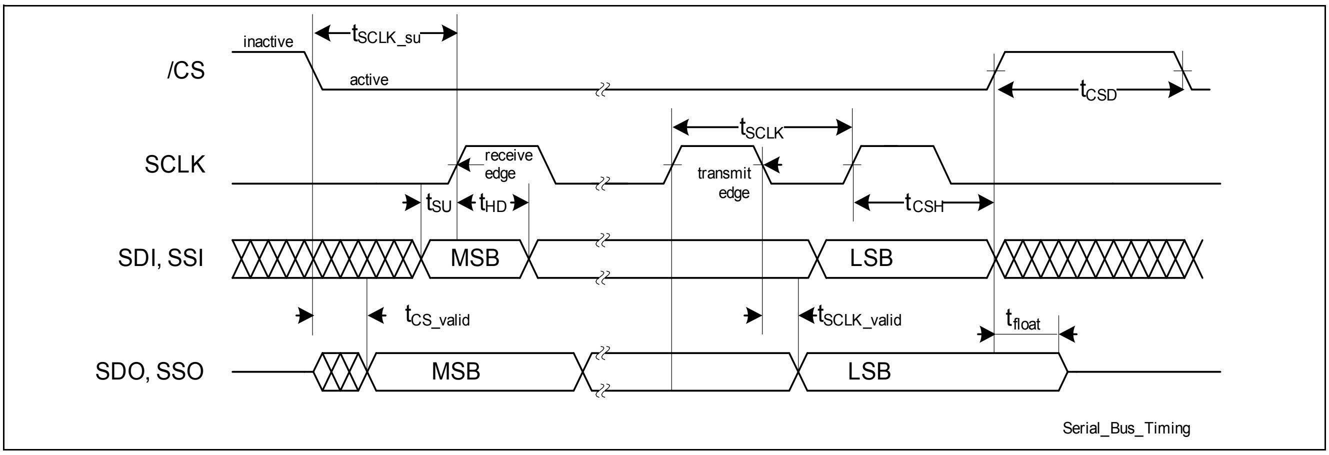



**Figure 22 Serial Bus Timing**

Several SPI topologies are supported: pure bus topology, daisy-chain and any combinations (**Figure 23**). Of course independent individual control with dedicated SPI controller interfaces for each slave IC is possible, as well.

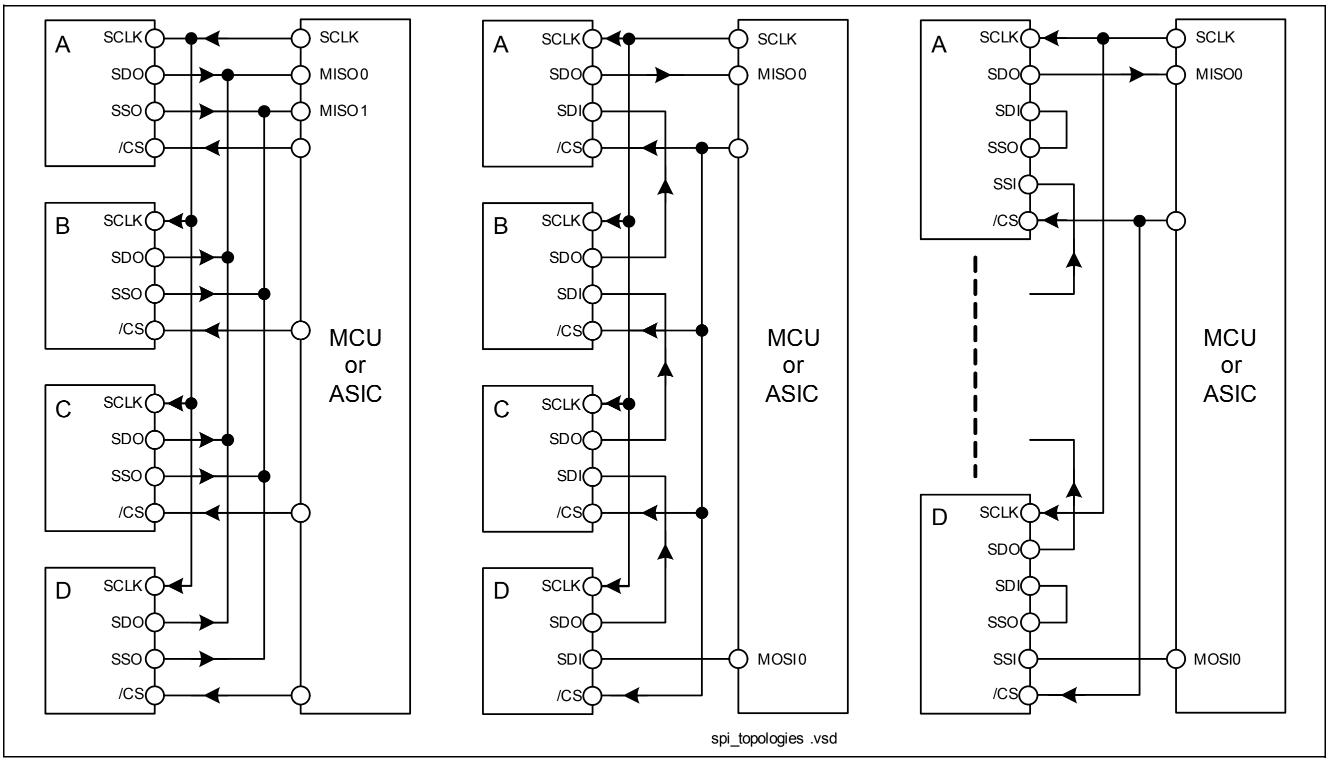



**Figure 23 Example SPI Topologies**

### 3.8.1 SPI Modes

The architecture provides 2 independent SPI-interfaces with serial read and serial write options. All register addresses can be accessed independently from both SPI-interfaces with one restriction : a simultaneous serial write on both SPI-interfaces is forbidden. Therefore only one temporary register for storing the write data is provided. All other combinations read (SPI_channel 1) / read (SPI_channel 2) and write (SPI_channel 1) / read (SPI_channel 2) and read (SPI_channel 1) / write (SPI_channel 2) are allowed. There are no restrictions on the selection of register addresses from both channels.

Write commands are configured with the MSB of the addess-byte set to “1”, read commands are configured with the MSB of the address-byte set to “0”.

#### 3.8.1.1 Switching Serial Modes

All serial modes MS1, MS0 = 11, 01, 10, 00 are switchable during operation but not within a serial transfer frame. No internal registers are affected. Only multiplexers and CRC-engines can be activated or deactivated. Internal FSMs are reset. The user has to run one dummy serial process after switching of a serial mode to clear the serial shift registers and reset the internal FSMs. For example: switching from MS1, MS0 = 00 to MS1, MS0 = 11 means the 24 bit serial shift registers and the CRC-engines will be activated. To guarantee proper operation one dummy read sequence has to be processed means “shift in 24 bits with read address, zeros and CRC within a $\overline{CS}$= Low frame” to operate the serial interface in the new mode. A reliable output is not guaranteed for the first serial process. The same is true for changing the serial mode in the reverse direction : from MS1, MS0 = 11 to MS1, MS0 = 00. Here at least one dummy serial access (8 SCLK-cycles) within a $\overline{CS}$=Low frame is necessary.

Be aware that in Mode01 read access the date at SDO/SSO corresponds to the adress which has been written in the frame before. Mode00 and Mode 01 support the daisy-chain application.

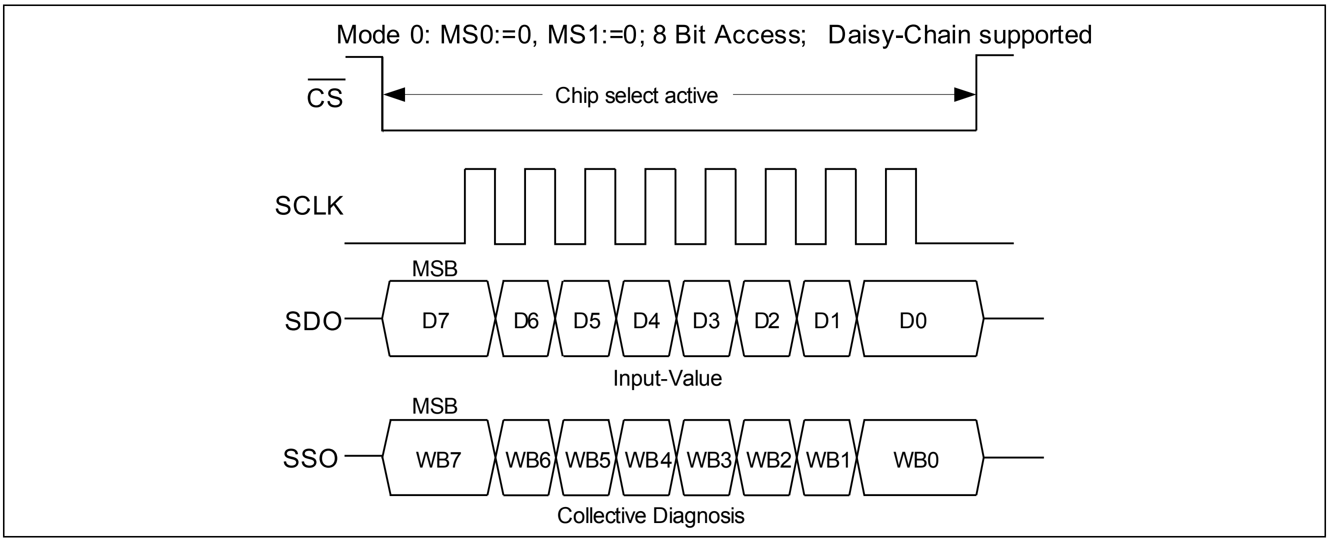



**Figure 24 SPI Mode 0**

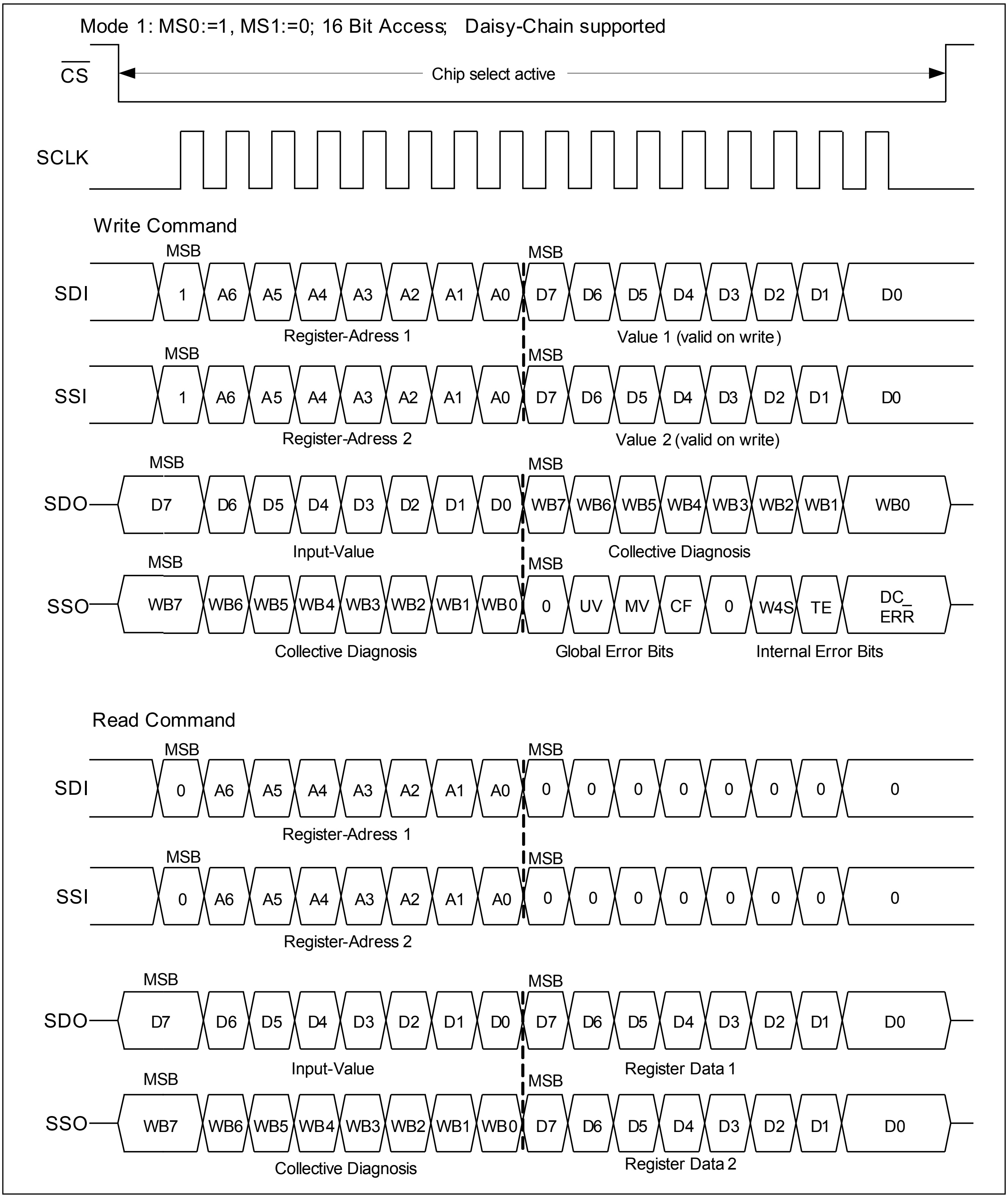



**Figure 25 SPI Mode 1**

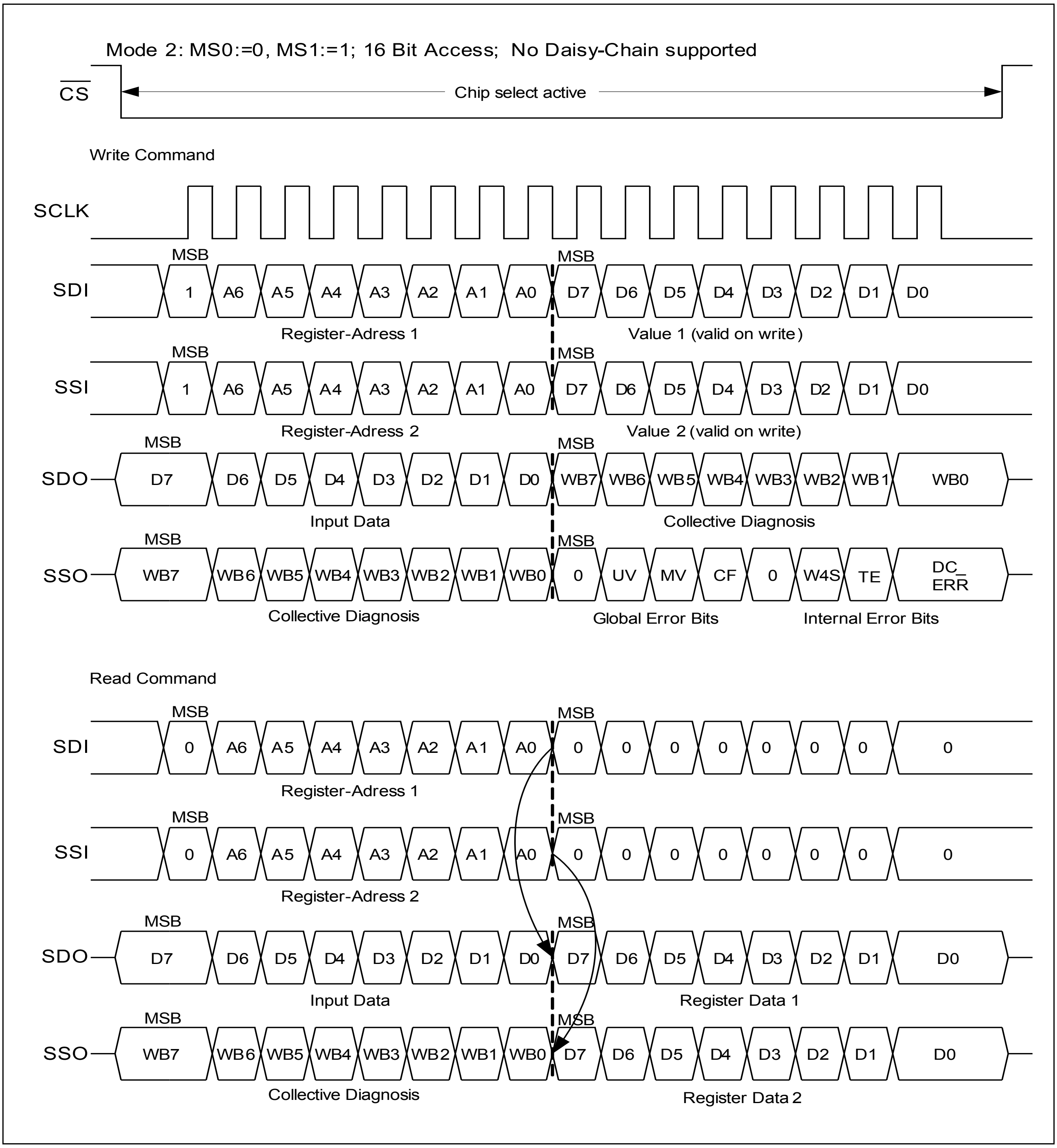



**Figure 26 SPI Mode 2**

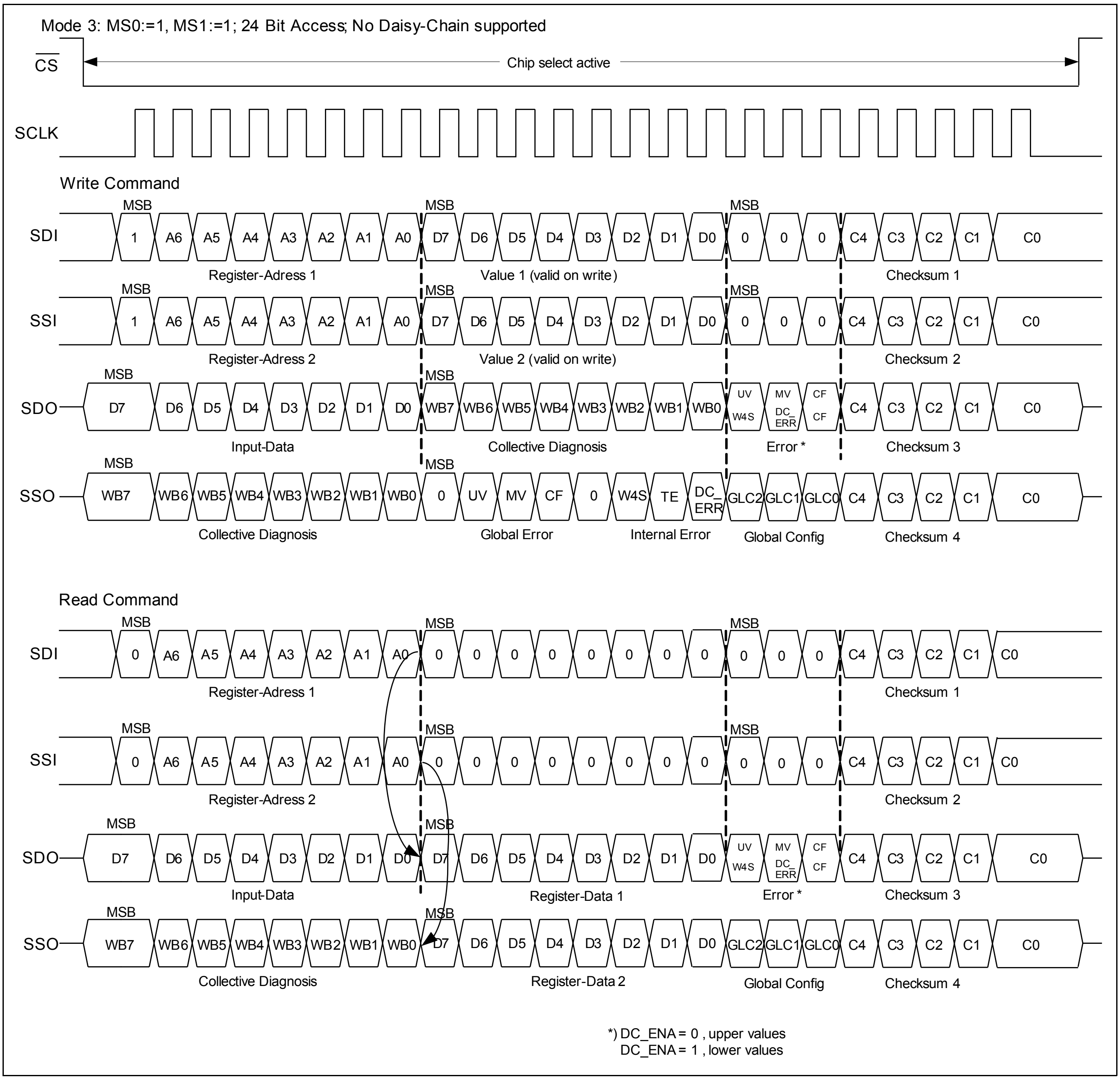



**Figure 27 SPI Mode 3**

The error values in the SDO-segment depends on the setting of DC_ENA. If DC_ENA is set to ‘1’ the IC is supplied by the integrated DC/DC converter and the error information W4S, DC_ERR, CF is valid. If DC_ENA is set to ‘0’ the error information UV, MV, CF is valid

### 3.8.2 Architecture of CRC-Engines

For writing serial data into the uC-interface chip one serial-SPI-mode (MS1, MS0 = 11) delivers with the pure input data bit stream (write by an uC, 19 bits ) also the CRC-signature (5 bits). The total bitstream is fed into the CRC-input engines and processed according to the underlying CRC-algorithm serially.

The CRC is a 5-Bit-checksum and will be calculated with the polynom X5+ X4+ X2+1 and is calculated from Bit [23:5]. The checksum is transfered to Bit [4:0]. After totally processed 24 serially shifted in-bits (including the CRC-signature) the total result of the CRC-algorithm processing has to be zero. In the case of another result different from zero the delivered signature is not consistent with the delivered bit stream. This will be indicated by setting the CRC_ERR Pin to Low.

For reading of registers by a uC a CRC-signature (5 bits) (MS1, MS0 = 11) will be delivered with the pure data bit stream (19 bits) : data output (read by a uC). The read bitstream has to be processed according to the CRC-algorithm serially. After totally processed 19 serially shifted out-bits the CRC-signature has been calculated and delivered to the output pins SDO, SSO.

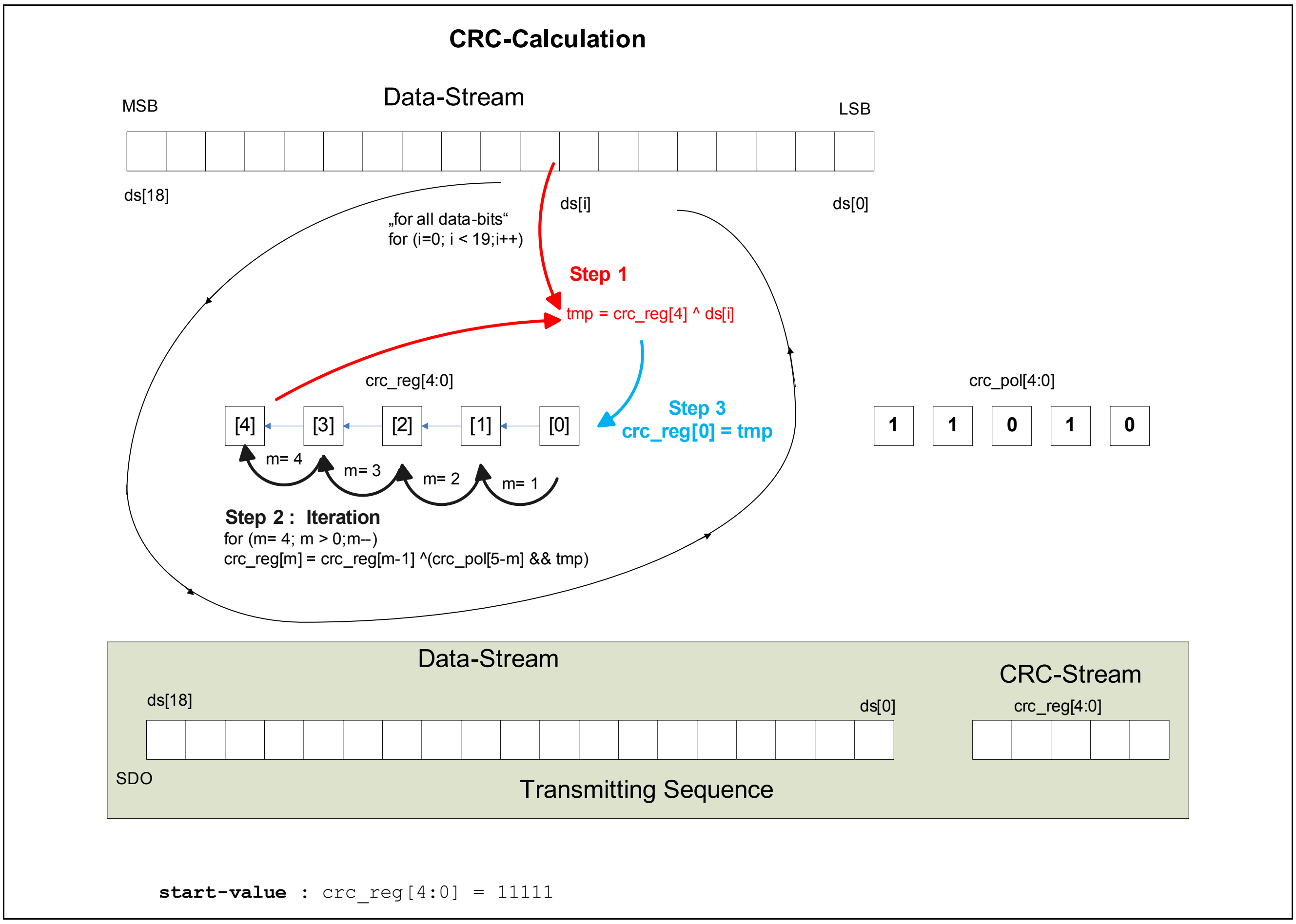



Figure 28 CRC-Calculation

## 3.9 SYNC Operation

In automation systems there is sometimes the need to actualize the input-signal/collective diagnostics at the same time system-wide. Therefore a signal SYNC is needed to latch the input-signals/collective diagnostics at the given time, otherwise the input-signals/collective diagnostics have to be actualized continously with the system clock clk_500k.

The filtered data and diagnostics can be synchronized on the falling edge of the SYNC pin or "frozen" by holding SYNC Low (see **Figure 29** and **Table 17**).

The filtered input data will be latched in the input-value-register and the filtered wire-break diagnosis (inclusive CF-bit) will be latched into the collective diagnosis register every data-cycle when the SYNC-signal is in high state or with the falling edge of SYNC . When the SYNC-signal is in low state the input-data-register and the collective diagnosis register won't be updated any longer. In the same way the SYNC-signal actualizes the information of the global and internal error register.

The SYNC-signal doesnot affect the operation of the internal filtering-structures.

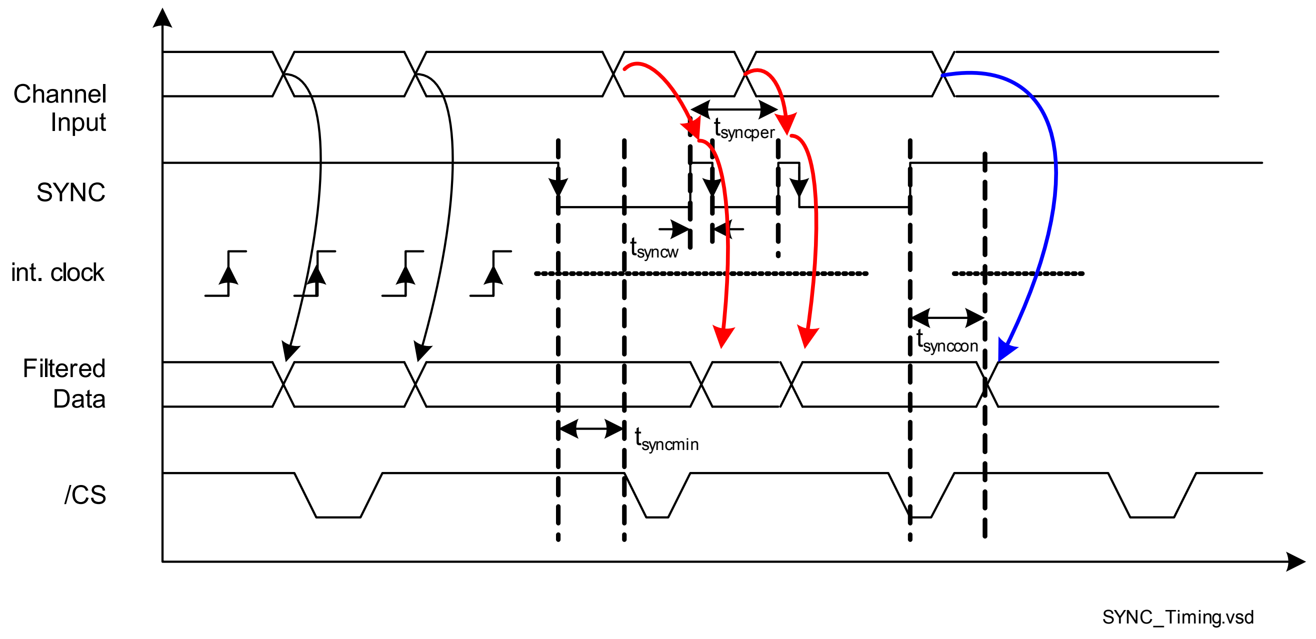



**Figure 29 SYNC Operation Timing**

## 3.10 Write-Read- Access and Read-Read-Access for Different Applications

Depending on the application different timing requirements on the $\overline{CS}$-idle cycle ($\overline{CS}$ = high) or on the $\overline{CS}$-period have to be obeyed ( **Figure 30** ). The parameters are specified in the electrical requirements. The verification of the parameter $t_{RD\_PER}$ is performed in the way that a wirebreak signal for 4 usec is generated, after the propagation delay over the sense chip and the CT the corresponding DIAG-bit (plus an uncertainty of +- 1 cycle ($f_{scantyp}$ )) has to be detected. After reading the DIAG-register it has to be assured that the DIAG-register has been cleared (after about 2 cycles with an uncertainty of +- 1 cycle ($f_{scantyp}$ )).

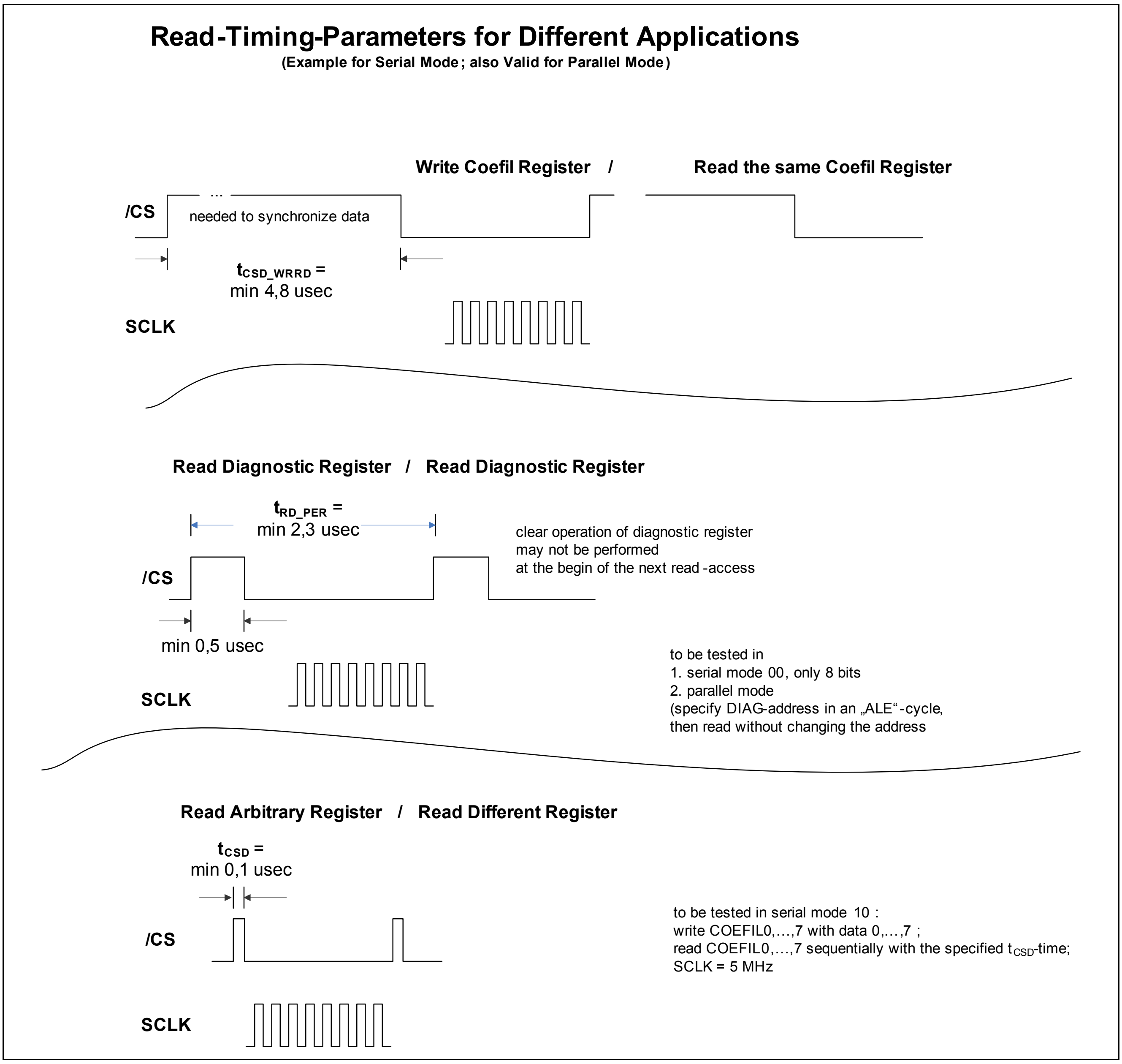



**Figure 30 Critical Timing Parameters for Write-Read-Access or Read-Read-Access**

# 4 Standard Compliance

The ISO1I813T allows the design of a sensor interface compliant with the standard requirements listed below:

System Insulation Characteristics as shown in **Table 3**,

System Immunity Characteristics as shown in **Table 5**.

There requirements are valid for an application using the ISO1I813T including external circuitry (as proposed in **Figure 31**), not for the IC alone.

*Note: When the IC is not supplied, probing of the digital input interface is still possible due to the external circuitry, i.e. the 12k resistor and the LED. In addition to the current through the LED a small current $I_{IxH}$ flows through the pins IxH and IxL.*

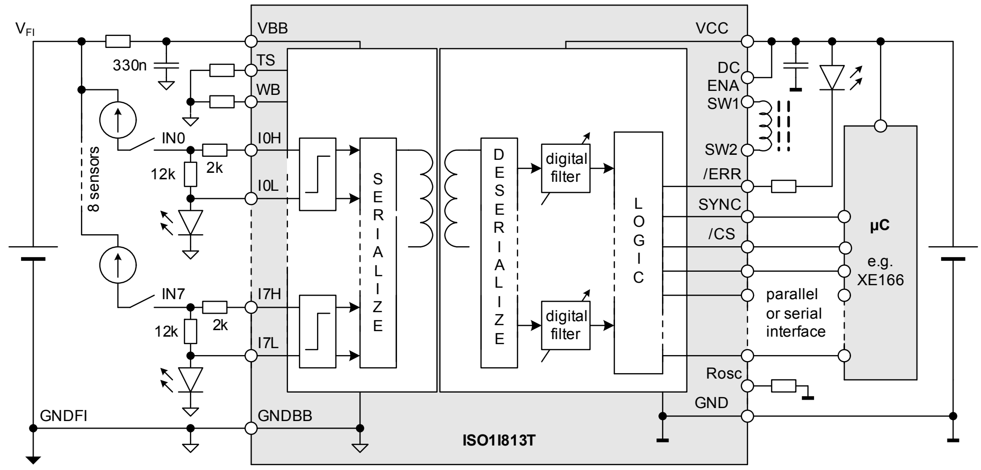



**Figure 31 Recommended Application Circuit**

**Table 2 System Absolute Maximum Ratings**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Field Input Voltage Overvoltage 1300 ms | $V_{FIov}$ | -45 | | +45 | V | |
| Input Voltage INx | $V_{INx}$ | -45 | | +45 | V | |

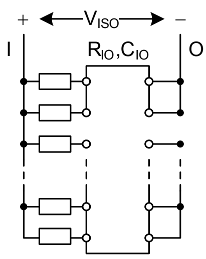



**Figure 32 System Insulation Characteristics**

**Table 3 System Insulation Characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Pollution Degree (DIN VDE 0110/1.89, DIN EN 60664-1) | | | 2 | | | |
| Minimum External Clearance | CLR | 6.7 | | | mm | |
| Minimum External Creepage | CPG | 6.2 | | | mm | |
| Maximum Working Insulation Voltage | $V_{ISO}$ | 500 | | | $V_{AC}$ | 1 min duration[1)] |

1) not subject to production test, verified by characterization

**Approvals:**

UL1577

Certificate Number 20120309-E311313

# 5 Electrical Characteristics

This section comprises:

- Operating Conditions and Power Supply (see **Chapter 5.2**)
- Electrical Characteristics Input Side (see **Chapter 5.3**)
- Electrical Characteristics Microcontroller Interface (see **Chapter 5.4**)

Tolerance values always contain the sum of process-related tolerance values and tolerance-values based on the temperature drift within the specified temperature range.

## 5.1 Absolute Maximum Ratings

All voltages at pins 25 to 48 are measured with respect to ground GNDBB. All voltages at pins 1 to 24 are measured with respect to GND. The voltage levels are valid if other ratings are not violated. The two voltage domains VCC, GND and VBB, GNDBB are internally electrically isolated.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4 Absolute Maximum Ratings**

| Parameter | Symbol | Value | | Unit | Note / Test Condition |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Continuous Voltage at pin VBB | $V_{VBB}$ | -0.3 | 45 | V | Power Dissipation must not exceed max-value |
| Peak Voltage VBB, Overvoltage 500 ms | $V_{VBB}$ | -0.3 | 45 | V | |
| Supply Voltage VCC | $V_{VCC}$ | -0.3 | 6.5 | V | |
| Continuous Voltage at logic pins 1 - 24 (except VCC and GND pins) | $V_{LOG}$ | -0.3 | 6.5 | V | |
| Continuous Voltage at pin TS, WB | | -0.3 | 6.5 | V | |
| Junction Temperature | $T_J$ | -40 | 150 | °C | |
| Storage Temperature | $T_S$ | -50 | 150 | °C | |
| Power Dissipation | $P_{tot}$ | | 800 | mW | |
| Input Voltage Range | $V_{IxH}$ | -45 | 45 | V | |
| Input Voltage Range | $V_{IxL}$ | -0.3 | 5 | V | |
| Error Pin Sink Current ($\overline{ERR}$=0) | $I_{ERRsink}$ | | 5 | mA | $V_{ERR} < 0.25 \cdot V_{VCC}$ |
| Error Pin Sink Current ($\overline{CRCERR}$=0) | $I_{CRCsink}$ | | 5 | mA | $V_{ERR} < 0.25 \cdot V_{VCC}$ |
| DC-DC switch outputs 1/2 | SW1/2 | | 20 | V | |
| Electrostatic discharge voltage (Human Body Model) according to JESD22-A114-B | $V_{ESD}$ | – | – | 2.5 | kV |
| Electrostatic discharge voltage (Charge Device Model) according to ESD STM5.3.1 - 1999 | $V_{ESD}$ | – | – | 1.5 | kV |

## 5.2 Operating Conditions and Power Supply

For proper operation of the device, absolute maximum rating (**Chapter 5.1**) and the parameter ranges in **Table 5** must not be violated. Exceeding the limits of operating condition parameters may result in device malfunction or spec violations. The power supply pins VBB and VCC have the characteristics given in **Table 7**.

**Table 5 Operating Range**

| Parameter<br>at $T_j$ = -40 ... 125°C | Symbol | Value | | Unit | Note / Test Condition |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Supply Voltage Logic VCC | $V_{VCC}$ | *2.85* | 5.5 | V | related to GND |
| Supply Voltage Senses VBB | $V_{VBB}$ | *9.6* | 35 | V | related to GNDBB |
| Continuous VBB Voltage in Self-Power Mode | $V_{VBBDC}$ | 12 | 16 | V | see **Figure 5** and **Table 8** for operation points[1)] |
| Ambient Temperature | $T_A$ | -40 | 85 | °C | |
| Junction Temperature | $T_J$ | -40 | 125 | °C | |
| Common Mode Transient | $dV_{ISO}/dt$ | -25 | 25 | kV/µs | |
| Magnetic Field Immunity | $\|H_{IM}\|$ | 30 | | A/m | IEC61000-4-8 |

1) recommended for operation

**Table 6 Thermal Characteristics**

| Parameter<br>at $T_j$ = -40 ... 125°C, $V_{bb}$=9.6...35V, $V_{CC}$=2.85...5.5V, unless otherwise specified | Symbol | Limit Values | | Unit | Note / Test Condition |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Thermal resistance junction - case top | $R_{thJC\_Top}$ | | 15.0. | K/W | measured on top side[1)] |
| Thermal resistance junction - case bottom | $R_{thJC\_Bot}$ | | 13.8. | K/W | [1)] |
| Thermal resistance junction - pin | $R_{thJP}$ | | 11.8 | K/W | [1)] |
| Thermal resistance @ 2 cm² cooling area[2)] (thermal conductance only by radiation and free convection) | $R_{th(JA)}$ | | 88.6 | K/W | [1)] |

1) not subject to production test, specified by design
2) Device on 50 mm x 50 mm x 1.5 mm epoxy PCB FR4 with 2 cm² (one layer, 35 µm thick) copper area. PCB is vertical without blow air.

**Table 7 Electrical Characteristics of the Power Supply Pins**

| Parameter<br>at $T_j$ = -40 ... 125°C, $V_{bb}$=9.6...35V, $V_{CC}$=2.85...5.5V, unless otherwise specified | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| VBB UVLO startup threshold | $V_{VBBon}$ | | | 9.6 | V | |
| VBB UVLO shutdown threshold | $V_{VBBoff}$ | 8.0 | | | V | [1)] |
| VBB UVLO Hysteresis | $V_{VBBhys}$ | | 1 | | V | |
| VBB missing voltage OFF (MV) threshold | $V_{VBBmvoff}$ | | | 13.9 | V | |

**Table 7 Electrical Characteristics of the Power Supply Pins** (cont'd)

| Parameter at $T_j$ = -40 ... 125°C, $V_{bb}$=9.6...35V, $V_{CC}$=2.85...5.5V, unless otherwise specified | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| VBB missing voltage ON (MV) threshold | $V_{VBBmvon}$ | 12.1 | | | V | |
| VBB undervoltage OFF (UV) threshold | $V_{VBBuvoff}$ | | | 17.0 | V | |
| VBB undervoltage voltage ON (UV) threshold | $V_{VBBuvon}$ | 15.0 | | | V | |
| Glitch filters for VBB missing voltage and undervoltage | $T_{VBBfil}$ | | 8 | | µs | 2) |
| Undervoltage Current for VBB | $I_{VBBuv}$ | | 3.5 | | mA | $V_{VBB} < V_{VBBon}$ |
| Quiescent Current VBB | $I_{VBBq}$ | | 5 | | mA | $V_{VBB}$ = 24 V, $I_{INx}$ = 0, VCC = 0V |
| Startup Delay (time between VBBon/VCCon and first data output) | $t_{VXXon}$ | | 26 | | µs | Digital Filter bypassed 2) 3) |
| VCC UVLO startup threshold | $V_{VCCon}$ | | | 2.85 | V | |
| VCC UVLO shutdown threshold | $V_{VCCoff}$ | 2.5 | | | V | 4) |
| VCC UVLO threshold hysteresis | $V_{VCChys}$ | | 0.1 | | V | |
| Quiescent Current VCC | $I_{VCCq}$ | | 3.1 | | mA | $V_{VCC}$ = 5 V 2) 5) $V_{VBB}$ = 0V |
| Quiescent Current VCC | $I_{VCCq}$ | | 2.3 | | mA | $V_{VCC}$ = 3.3 V 2) 5) $V_{VBB}$ = 0V |

1) Note that the specified operation of the IC requires $V_{VBB}$ as given in **Table 5**
2) defined for $f_{scantyp}$ 500kHz
3) not subject to production test, specified by design
4) Note that the specified operation of the IC requires $V_{VCC}$ as given in **Table 5**
5) No Push-Pull Converter connected at SW1/2

**Table 8 Self-Powered Supply Operation**

| Parameter at $T_j$ = -40 ... 125°C, $V_{bb}$=9.6...35V, $V_{CC}$=2.85...5.5V, unless otherwise specified | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ON Resistance at SW1/2 | $R_{DSON}$ | | | 2.3 | Ω | 140 mA |
| Current Rating | $I_{SW}$ | | | 140 | mA | |
| Thermal overload trip temperature | $T_{jt}$ | 157 | | 165 | °C | 1) |
| Thermal hysteresis | $\Delta T_{jt}$ | | 5 | | K | 1) |

1) not subject to production test, specified by design

## 5.3 Electrical Characteristics Input Side

The electrical characteristics of the input side (pins 25-48) are given in **Table 9**. Note that some parameters refer to IN0 to IN7 which are nodes of external circuitry (see **Figure 10** or **Figure 31**). Electrical characteristics with respect to these nodes are given for the system including the external circuitry and not for the IC alone.

See also **Figure 11** for the different threshold parameters.

**Table 9 Sensors Inputs**

| **Parameter** at $T_j$ = -40 ... 125°C, $V_{bb}$=9.6...35V, $V_{CC}$=2.85...5.5V, unless otherwise specified | **Symbol** | **Values** | | | **Unit** | **Note / Test Condition** |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | |
| Sink Current Limit at Saturation Edge Type 1/3 | $I_{INxsnkC13}$ | 2.3 | | | mA | $V_{VBB}$=$V_{VBBon}$, $V_{INx}$=6.7V, $V_{IxL}$=1.2V |
| Sink Current Limit at Saturation Edge Type 2 | $I_{INxsnkC2}$ | 3.3 | | | mA | $V_{VBB}$=$V_{VBBon}$, $V_{INx}$=6.7V, $V_{IxL}$=1.2V |
| Sink Current Limit at Maximum Input Voltage Type 1/3 | $I_{INxsnkM13}$ | | | 3.4 | mA | $V_{VBB}$=35V, $V_{INx}$=30V, $V_{IxL}$=2.5V |
| Sink Current Limit at Maximum Input Voltage Type 2 | $I_{INxsnkM2}$ | | | 4.8 | mA | $V_{VBB}$=35V, $V_{INx}$=30V, $V_{IxL}$=2.5V |
| LED Supply Current at Maximum Input Voltage, Type 1/3 | $I_{IxLmax}$ | 2.1 | | 3.1 | mA | $V_{VBB}$=35V, $V_{INx}$=30V, $V_{IxL}$=2.5V |
| LED Supply Current at Maximum Input Voltage, Type 2 | $I_{IxLmax}$ | 3.1 | | 4.5 | mA | $V_{VBB}$=35V, $V_{INx}$=30V, $V_{IxL}$=2.5V |
| LED Supply Current at High Threshold Type 3 | $I_{IxL3}$ | 1.5 | | 2.5 | mA | $V_{VBB}$=$V_{VBBon}$, $V_{INx}$=11V, $V_{IxL}$=2.5V |
| LED Supply Current at High Threshold Type 2 | $I_{IxL2}$ | 2.3 | | 3.6 | mA | $V_{VBB}$=$V_{VBBon}$, $V_{INx}$=11V, $V_{IxL}$=2.5V |
| LED Supply Current at High Threshold Type 1 | $I_{IxL1}$ | 1.6 | | 2.6 | mA | $V_{VBB}$=$V_{VBBon}$, $V_{INx}$=15V, $V_{IxL}$=2.5V |
| LED Voltage recommended | $V_{FLED}$ | 1.9 | | 3.0 | V | 1) |
| Sense Voltage Switching Threshold, L→H (Type 1) | $V_{INxDset(1)}$ | | | 15 | V | $V_{VBB}$=24V $V_{IxL}$=2.5V 2) |
| Sense Voltage Switching Threshold H→L (Type 1) | $V_{INxDclr(1)}$ | 11 | | | V | $V_{VBB}$=24V $V_{IxL}$=2.5V 2) |
| Hysteresis H↔L (Type 1) | $V_{INxDhys(1)}$ | | 1 | | V | |
| Sense Voltage Switching Threshold L→H (Type 2) | $V_{INxDset(2)}$ | | | 11 | V | $V_{VBB}$=24V $V_{IxL}$=2.5V 2) |
| Sense Voltage Switching Threshold H→L (Type 2) | $V_{INxDclr(2)}$ | 7 | | | V | $V_{VBB}$=24V $V_{IxL}$=2.5V 2) |
| Hysteresis H↔L (Type 2) | $V_{INxDhys(2)}$ | | 0.65 | | V | |
| Sense Voltage Switching Threshold L→H (Type 3) | $V_{INxDset(3)}$ | | | 11 | V | $V_{VBB}$=24V $V_{IxL}$=2.5V 2) |
| Sense Voltage Switching Threshold H→L (Type 3) | $V_{INxDclr(3)}$ | 7 | | | V | $V_{VBB}$=24V $V_{IxL}$=2.5V 2) |

**Table 9 Sensors Inputs** (cont'd)

| **Parameter** at $T_j$ = -40 ... 125°C, $V_{bb}$=9.6...35V, $V_{CC}$=2.85...5.5V, unless otherwise specified | **Symbol** | **Values** | | | **Unit** | **Note / Test Condition** |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | |
| Hysteresis H↔L (Type 3) | $V_{INxDhys(3)}$ | | 0.7 | | V | |
| Input Sink Current when $V_{VBB}$=0 | $I_{IxHq}$ | | 300 | | µA | $V_{VBB}$=0V<br>$V_{IxH}$=30V , IxI = open |

1) not subject to production test, specified by design
2) clamped to 2.5V if "logic 1", internally limited if logic "0"

**Table 10 Setting at the Configuration Pins (TS, WB)**

| **Parameter** at $T_j$ = -40 ... 125°C, $V_{bb}$=9.6...35V, $V_{CC}$=2.85...5.5V, unless otherwise specified | **Symbol** | **Values** | | | **Unit** | **Note / Test Condition** |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | |
| TS Pull-Down Resistance for Type 1 Selection | $R_{TSpd1}$ | | 33 | | Ω | 1) |
| TS Pull-Down Resistance for Type 2 Selection | $R_{TSpd2}$ | | 33 | | kΩ | 1) 2) |
| TS Pull-Down Resistance for Type 3 Selection | $R_{TSpd3}$ | | 330 | | kΩ | 1) |
| WB pin source current | $I_{WBsource}$ | | 12.5 | | µA | $R_{WB}$ = 40kΩ |
| WB pin detection current | $I_{WB}$ | | 80 | | µA | $R_{WB}$ = 40kΩ |
| Wirebreak detection blanking time | $t_{WB\_blank}$ | | 1 | | µs | 3) 4) |
| Type selection blanking time | $t_{TS\_blank}$ | | 2 | | µs | 3) 4) |
| Max. WB Pin Load Capacitance | $C_{WBmax}$ | | | 5 | pF | 1) |
| Max. TS Pin Load Capacitance | $C_{TSmax}$ | | | 20 | pF | 1) |

1) required for operation
2) Only 4 channels can be used for this case.
3) not subject to production test, specified by design
4) defined for $f_{scantyp}$ 500kHz

## 5.4 Electrical Characteristics Microcontroller Interface

For the Parallel Mode see **Table 11**, **Table 12**, **Table 14** and **Table 15**,

For the Serial Mode see **Table 11**, **Table 12**, **Table 14** and **Table 16**.

Timing characteristics refer to $C_L$ < 50 pF and $R_L$ > 10 kΩ.

**Table 11 Sensor Scanning and Averaging** [1)]

| Parameter at $T_j$ = -40 ... 125°C, $V_{bb}$=9.6...35V, $V_{CC}$=2.85...5.5V, unless otherwise specified | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Typical Scan Frequency | $f_{scantyp}$ | 440 | | 510 | kHz | $R_{OSC}$ = 22.1 kΩ without tolerance |
| Scan Frequency Range | $f_{scanrge}$ | 50 | | 500 | kHz | [2)] refer to **Figure 8** |
| Input Scan Propagation Delay | $t_{ctdelay}$ | | 8 | | µs | [1)] applies equally to all channels |
| Filter Bypass delay | $t_{bypass}$ | | 2 | | µs | [1)] |
| Minimal Filter Output valid time (until Readout i.e. $\overline{CS}$ falling edge) | $t_{csrdy}$ | | 1.2 | | µs | including maximum channel jitter [1)] |
| Channel Jitter[3)] | $t_{chnjitter}$ | 0 | | 2 | µs | for $t_{FILT00}$ and $t_{FILT01}$ [1)] |
| Channel Jitter | $t_{chnjitter}$ | 0 | | 1.5 | % | for $t_{FILT02}$ to $t_{FILT07}$ [1)] |
| Default Digital Filter Monitoring Time | $t_{FILTdef}$ | | 4 | | us | bypass[1))] |
| Digital Filter Monitoring Time | $t_{FILT00}$ | | 0.050 | | ms | FT=$00_H$ [1)] |
| Digital Filter Monitoring Time | $t_{FILT01}$ | | 0.100 | | ms | FT=$01_H$ [1)] |
| Digital Filter Monitoring Time | $t_{FILT02}$ | | 0.400 | | ms | FT=$02_H$ [1)] |
| Digital Filter Monitoring Time | $t_{FILT03}$ | | 0.800 | | ms | FT=$03_H$ [1)] |
| Digital Filter Monitoring Time | $t_{FILT04}$ | | 1.600 | | ms | FT=$04_H$,prescaler used[1)] |
| Digital Filter Monitoring Time | $t_{FILT05}$ | | 3.200 | | ms | FT=$05_H$, prescaler used[1)] |
| Digital Filter Monitoring Time | $t_{FILT06}$ | | 10.000 | | ms | FT=$06_H$, prescaler used[1)] |
| Digital Filter Monitoring Time | $t_{FILT07}$ | | 20.000 | | ms | FT=$07_H$, prescaler used[1)] |
| Digital Filter Monitoring Time | $t_{FILToff}$ | | 4.0 | | µs | FT=$08_H$..$0F_H$ [1)] |

1) valid for $f_{scantyp}$ = 500kHz
2) not subject to production test, specified by design
3) the channel jitter is defined in **Figure 18**

**Table 12 Setting at the Configuration Pin (Rosc) see also Figure 8**

| Parameter<br>at $T_j$ = -40 ... 125°C, $V_{bb}$=9.6...35V, $V_{CC}$=2.85...5.5V, unless otherwise specified | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Rosc Pin Source Current | $I_{Roscsrc}$ | | 50 | | µA | $R_{OSC}$ = 22.1 kΩ |
| Rosc Resistance to GND | $R_{Rosc}$ | 18.4 | 22.1 | 221 | kΩ | E96 resistor |
| Rosc Pin Regulated Voltage | $V_{Roscreg}$ | | 1.2 | | V | |
| Max. Rosc Pin Load Capacitance | $C_{Roscmax}$ | | | 5 | pF | 1) |

1) required for operation

**Table 13 Error Pins ($\overline{ERR}$, $\overline{CRCERR}$)**

| Parameter<br>at $T_j$ = -40 ... 125°C, $V_{bb}$=9.6...35V, $V_{CC}$=2.85...5.5V, unless otherwise specified | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Error Pin Pull-Up Resistance ($\overline{ERR}$=1) | $R_{ERRpu}$ | | 50 | | kΩ | |
| Maximum Switching Frequency ($\overline{ERR}$, $\overline{CRCERR}$) | $f_{SW}$ | 10 | | 500 | kHz | 1) |
| Error Pin Low voltage | $V_{ERROL}$ | | | $0.25 \cdot V_{VCC}$ | V | $I_{ERROL}$ = 5mA |

1) not subject to production test, specified by design

**Table 14 Logical Pins ($\overline{RD}$, $\overline{WR}$, ALE, MS0/1, $\overline{CS}$, AD7:AD0, SCLK, SDO, SSO, SDI, SSI, SEL)**

| Parameter<br>at $T_j$ = -40 ... 125°C, $V_{bb}$=9.6...35V, $V_{CC}$=2.85...5.5V, unless otherwise specified | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input Voltage High Level | $V_{IH}$ | $0.7 \cdot V_{VCC}$ | | $V_{VCC}+0.3$ | V | |
| Input Voltage Low Level | $V_{IL}$ | -0.3 | | $0.3 \cdot V_{VCC}$ | V | |
| Input Voltage Hysteresis | $V_{Ihys}$ | | 100 | | mV | |
| Output Voltage High Level | $V_{OH}$ | $0.75 \cdot V_{VCC}$ | | $1 \cdot V_{VCC}$ | V | $I_{OH}$ = 5mA |
| Output Voltage Low Level | $V_{OL}$ | 0 | | $0.25 \cdot V_{VCC}$ | V | $I_{OL}$ = 5mA |
| Output Voltage High Level | $V_{OH}$ | | 2.75 | | V | $V_{VCC}$ = 2,85 V, $I_{OH}$ = 1mA 1) |
| Output Voltage Low Level | $V_{OL}$ | | 0.1 | | V | $V_{VCC}$ = 2,85 V - 5,5 V, $I_{OL}$ = 1mA |

1) Typical values over temperature derived with IOH = 5 mA and IOL = 5 mA ; extrapolated to IOH = 1mA and IOL = 1mA according to simulation results, voltage drop scales with a factor of 1/5 with the change of 5 mA to 1 mA, not subject to production test

**Table 15 Parallel Interface**

| Parameter<br>at $T_j$ = -40 ... 125°C, $V_{bb}$=9.6...35V, $V_{CC}$=2.85...5.5V, unless otherwise specified | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input Pull Up Resistance ($\overline{RD}$, $\overline{WR}$, $\overline{CS}$) | $R_{PU}$ | | 50 | | kΩ | |
| Input Pull Down Resistance (ALE) | $R_{PD}$ | | 50 | | kΩ | |
| Read Request Frequency | $f_{RD}$ | 0.06 | | 5 | MHz | repeated read access during $\overline{CS}$ = 0 |
| Read Request Period (1/$f_{RD}$) | $t_{RD}$ | 200 | | 15000 | ns | repeated read access during $\overline{CS}$ = 0 |
| $\overline{CS}$ Disable time ($\overline{CS}$ high time between two read accesses on different registers)[1)] | $t_{CSD}$ | 100 | | | ns | |
| Read-Period for two read accesses on the same register (especially for DIAG, GLERR,INTERR)[2)] | $t_{RD\_PER}$ | 2300 | | | ns | defined for $f_{scantyp}$ |
| $\overline{CS}$ Disable time ($\overline{CS}$ high time between a write access and a read access for reading back the written value) | $t_{CSD\_WRRD}$ | 4800 | | | ns | defined for $f_{scantyp}$ |
| AD0-7 Output valid by read | $t_{ADvalid}$ | | | 55 | ns | |
| /RD setup time | $t_{RD\_su}$ | 55 | | | ns | |
| /WR setup time | $t_{WR\_su}$ | 55 | | | ns | |
| /RD Low duration | $t_{RDlow}$ | 100 | | | ns | |
| /WR Low duration | $t_{WRlow}$ | 100 | | | ns | |
| /RD hold time | $t_{RD\_hd}$ | 0 | 20 | | ns | |
| /WR hold time | $t_{WR\_hd}$ | 0 | 20 | | ns | |
| /WR latency time | $t_{lat}$ | 600 | | | ns | |
| /RD Pad to DIAG, GLERR and INTERR Registers Update (Bits Clearing) | $t_{clrrdy}$ | 4 | | 6.2 | µs | |
| AD0-7 Output disable time | $t_{float}$ | | | 80 | ns | |
| AD0-7 Data bus setup time | $t_{AD\_su}$ | 40 | | | ns | |
| AD0-7 Data bus hold time | $t_{AD\_hd}$ | 50 | | | ns | |

1) not subject to production test, specified by design, verified on subset of ICs,over temperature and supply voltage, read of COEFIL-registers alternatively (**Figure 30**)

2) not subject to production test, specified by design, verified on subset of ICs,over temperature and supply voltage, permanent read of DIAG-register with a frequency of 500 kHz, supervision of setting of wirebreak-signal and clearing by read (**Figure 30**)

**Table 16 Serial Interface**

| Parameter<br>at $T_j$ = -40 ... 125°C, $V_{bb}$=9.6...35V, $V_{CC}$=2.85...5.5V, unless otherwise specified | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input Pull Up Resistance ( $\overline{CS}$) | $R_{PU}$ | | 50 | | kΩ | |
| Input Pull Down Resistance (SCLK, SDI) | $R_{PD}$ | | 50 | | kΩ | |
| Serial Clock Frequency | $f_{SCLK}$ | | | 5 | MHz | |
| Serial Clock Period ($1/f_{SCLK}$) | $t_{SCLK}$ | 200 | | | ns | |
| Serial Clock High Period | $t_{SCLKH}$ | 100 | | | ns | |
| Serial Clock Low Period | $t_{SCLKL}$ | 100 | | | ns | |
| Minimum $\overline{CS}$ Hold time (rising edge of SCLK to rising edge of $\overline{CS}$) | $t_{CSH}$ | 40 | | | ns | |
| $\overline{CS}$ Disable time ($\overline{CS}$ high time between two read accesses on different registers)[1)] | $t_{CSD}$ | 100 | | | ns | |
| Read-Period for two read accesses on the same register (especially for DIAG, GLERR,INTERR)[2)] | $t_{RD\_PER}$ | 2300 | | | ns | defined for $f_{scantyp}$ |
| $\overline{CS}$ Disable time ($\overline{CS}$ high time between a write access and a read access for reading back the written value) | $t_{CSD\_WRRD}$ | 4800 | | | ns | defined for $f_{scantyp}$ |
| Minimum Data setup time (required time SDI to rising edge of SCLK) | $t_{SU}$ | 5 | | | ns | |
| Minimum Data hold time (rising edge of SCLK to SDI) | $t_{HD}$ | 15 | | | ns | |
| Minimum $\overline{CS}$ to SDO/SSO - Output valid time | $t_{CS\_valid}$ | 50 | | | ns | |
| /CS falling edge to first rising SCLK edge | $t_{SCLK\_su}$ | 80 | | | ns | |
| Minimum SCLK to SDO/SSO - Output valid time | $t_{SCLK\_valid}$ | | | 80 | ns | |
| Minimum SDO/SSO - Output disable time | $t_{float}$ | | | 65 | ns | |
| New serial mode activation time (MS0/MS1 change to earliest interface access) | $t_{MS\_rdy}$ | | 4 | | µs | no µController access allowed during the change[3)] [4)] |

1) not subject to production test, specified by design, verified on subset of ICs,over temperature and supply voltage, read of COEFIL-registers alternatively (**Figure 30**)

2) not subject to production test, specified by design, verified on subset of ICs,over temperature and supply voltage, permanent read of DIAG-register with a frequency of 500 kHz, supervision of setting of wirebreak-signal and clearing by read (**Figure 30**)

3) not subject to production test, specified by design

4) valid for $f_{scantyp}$ = 500kHz

**Table 17 Sync and Coefficient Update Timing**

| Parameter<br>at $T_j$ = -40 ... 125°C, $V_{bb}$=9.6...35V, $V_{CC}$=2.85...5.5V, unless otherwise specified | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Minimum time interval for µC-Read-Access after falling edge of SYNC-signal | $t_{syncmin}$ | | 500 | | ns | |
| Minimum time interval for switching from sync mode into the continuous mode | $t_{synccon}$ | 3 | | | µs | |
| Minimum width of SYNC-signal | $t_{syncw}$ | 200 | | | ns | |
| SYNC-period | $t_{syncper}$ | 500 | | | ns | |
| Minimal time interval between 2 write cycles for filter time programming | $t_{filwr}$ | 4 | | | µs | [1)] |
| Minimal time interval between a write cycle and a read back cycle for filter time programming | $t_{filrd}$ | 4 | | | µs | [1)] |
| Minimal time interval between a filter time write cycle and updated filter data freeze | $t_{filrdy}$ | 4 | | | µs | [1)] |

1) valid for $f_{scantyp}$ = 500kHz

# 6 Registers of Microcontroller-Interface-Chip

This chapter describes the µController Chip registers.

**Table 6-1 Register Bit Type Definition**

| Type | Symbol | Description |
|---|---|---|
| Read | r | The bit can be read |
| Read only, updated by hardware | h | The bit is updated by the device itself (for instance: sticky bit) |
| Write | w | The bit can be written |

## 6.1 µController Chip Registers Overview

The **Table 6-2** gives an overview of the µController Chip registers and their address.

**Table 6-2 Registers Summary**

| Short Name | Description | Access Rights[1)] | Address A7-A0 |
|---|---|---|---|
| **DIAG** | Collective Diagnostics Register (Wire-Break Detection) | rh | $00_H$ |
| **INPDATA** | Input Data Register (Input Channel Data) | rh | $02_H$ |
| **GLERR** | Global Error Register | rh | $04_H$ |
| COEFIL0 (**COEFIL0-7**) | Filter Time for the Data and the Diagnostics of Channel 0 | rw | $06_H$, $86_H$ |
| COEFIL1 | Filter Time for the Data and the Diagnostics of Channel 1 | rw | $08_H$, $88_H$ |
| COEFIL2 | Filter Time for the Data and the Diagnostics of Channel 2 | rw | $0A_H$, $8A_H$ |
| COEFIL3 | Filter Time for the Data and the Diagnostics of Channel 3 | rw | $0C_H$, $8C_H$ |
| COEFIL4 | Filter Time for the Data and the Diagnostics of Channel 4 | rw | $0E_H$, $8E_H$ |
| COEFIL5 | Filter Time for the Data and the Diagnostics of Channel 5 | rw | $10_H$, $90_H$ |
| COEFIL6 | Filter Time for the Data and the Diagnostics of Channel 6 | rw | $12_H$, $92_H$ |
| COEFIL7 | Filter Time for the Data and the Diagnostics of Channel 7 | rw | $14_H$, $94_H$ |
| **INTERR** | Internal Error Register | rh | $16_H$ |
| **GLCFG** | Global Configuration Register | rw | $18_H$ , $98_H$ |
| | Reserved | n.a. | other |

1) r=read-only, rw=read-write (timing restrictions apply), rh=read update by hardware

## 6.2 Presentation of the Registers

The µController side chip provides several 8-bit registers which can be accessed by the µController over the serial or parallel interface. Since those registers are located in the chip internal clock domain, the access is controlled by an internal arbiter processing the read / write requests as well as the synchronization requirements especially to freeze the internal registers when the isochronous mode is used (pin SYNC).

Some timing requirements apply to guarantee the data consistency provided to the µController (see Electrical Characterisitcs).

### 6.2.1 Sensor Registers

The sensor data and status (Wire-Break) detected at the channel inputs IxH/L by the sensor side chip are available in the **INPDATA** and **DIAG** registers respectively. The bits of the **DIAG** register have a sticky property i.e.once a wire-break condition has been detected (after the filter time), the respective bits remain set. A read access resets the sticky bits under the condition, that no wirebreak is detected anymore and no wirebreak information is pending at the filter outputs anymore. In the serial modes, both registers are per default driven out at the SDO/SSO outputs.

### 6.2.2 Status Registers

The **GLERR** and **INTERR** registers contains the status of the IC. **GLERR** monitors the application relevant parameters: undervoltage (UV), missing voltage (MV) and collective fault (CF) whereas **INTERR** indicates the status of internal signals important for the proper operation of the IC: wait for sense chip (W4S), transmission error (TE) and DC-DC error (DC_ERR) in case of self powered mode. Those registers can be read over the serial or parallel interface especially to identify the fault causing the error pin (ERR) to be pulled down. There are different options to read those registers: either through direct addressing (e.g. parallel mode) or through the telegram mode when the serial interface is selected where the bits are shifted out during the transaction.

The bits of the **GLERR** and **INTERR** registers have a sticky property and remains set as long as they are not cleared by a read access and the fault condition is not detected anymore. The **Table 6-3** presents which bits are cleared depending on the serial mode and the SPI channel. In the case of the parallel interface, the bits cleared are the ones whose address is contained in the internal ALE register. Only the bits having been read can be cleared. Since the bits are frozen when a read access is detected, it is guaranted that only these bits read over the serial or parallel interface can be cleared: if the status of the bits changes during the transaction, they will not be cleared.

**Table 6-3 Clear of the Sticky Bits by Serial Interface**

| | **Mode 0** | **Mode 1** | | **Mode 2** | | **Mode 3** | |
|---|---|---|---|---|---|---|---|
| **Read / Write** | **Read** | **Read** | **Write** | **Read** | **Write** | **Read** | **Write** |
| SPI channel-0 | n.a. | RDREG[1] | DIAG | RDREG[1] | DIAG | RDREG [1] UV, MV, W4S, DC_ERR [2] | DIAG UV, MV, W4S, DC_ERR [2] |
| SPI channel-1 | DIAG | DIAG RDREG[1] | DIAG UV, MV, W4S, TE, DC_ERR | DIAG RDREG[1] | DIAG UV, MV, W4S, TE, DC_ERR | DIAG RDREG[1] | DIAG UV, MV, W4S, TE, DC_ERR |

1) The bits of register which is being read (Direct addressing)

2) depends on setting of DC_ENA

### 6.2.3 Configuration Registers

The filter times of each channel can be programmed with the **COEFIL0-7** registers. Since the write access requires some time to update the internal registers, specific timing requirements apply especially between 2 successive programming operations. The **COEFIL0-7** registers define as well if the wire break detection should be masked or not in the **DIAG** register.

Only one of the COEFILx registers can be written at the same time (in serial mode only one SPI channel can be used). It is possible to program a filter time and simultaneously to read out another register e.g. another channel filter time.

Furthermore, the behaviour of the IC can be customized with the **GLCFG** register:

- The ratio of the switching frequency of the DC-DC ouput stage over the internal clock frequency set at the pin CLKADJ can be changed from 1:1 (default) to 2:1.
- A soft reset can be generated to clear the filter stages and reinitialize the data transmission between Sense side and µController side chips.
- The automatical clearing of the **DIAG** register can be disabled, when the register is read without direct addressing.

## 6.3 µController Registers Description

### 6.3.1 Collective Diagnostics Register

This register contains the filtered values of the Wire-Break detection of the channels 0 to 7.
This register can be read by the µController. The WB[x] are set with the occurence of a wire break at input line x and can only be cleared by a read operation of this register if the wire break is not detected anymore (sticky bits). As soon as one of those bits is set, the CF-bit of the **GLERR** is set as well.The **Chapter 6.2.2** explains the way the sticky bits are cleared.

**DIAG**
**Collective Diagnostics Register**

**(Address : $00_H$)** **Reset Value: $00_H$**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **WB7** | **WB6** | **WB5** | **WB4** | **WB3** | **WB2** | **WB1** | **WB0** |

rh

| Field | Bits | Type | Description |
|---|---|---|---|
| **WB[x]** | 7-0 | rh | **Channel Wire-Break Detected**<br>This bit indicates if a Wire-Break has been detected at the channel x.<br>$0_B$ No wire-break signal detected at channel x.<br>$1_B$ A wire-break condition has been detected at channel x. |

### 6.3.2 Input Channel Data Register

This register contains the filtered values of the input data detected at the channels 0 to 7.
This register can be read by the µController.

When the parallel interface is selected, the default address contained in the internal ALE register is the address of this register.

**INPDATA**
**Input Data Register**

**(Address : $02_H$ )** **Reset Value: $00_H$**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |

rh

| Field | Bits | Type | Description |
|---|---|---|---|
| **D[x]** | 7-0 | rh | **Input Channel Data**<br>This bit represents the input data detected at the pins IxH of the channel x depending on the sensor type selected.<br>$0_B$ Input Data below the input threshold.<br>$1_B$ Input Data above the input threshold. |

### 6.3.3 Global Error Register

This register contains the status of the IC parameters monitored during operation.
This register can only be read by the µController. The CF-bit is the OR-combination of all the bits of the **DIAG** register. The bits of this register are sticky and can only be cleared when the bits are read out and the faults are not detected anymore (refer to **Chapter 6.2.2** for more details).

The UV and MV bits are reset to 1 when the VBB voltage is below the UVLO threshold or during transmission error between the sensor side and µController side. The bits of the **GLERR** register are used in the generation of the signal of the error pin ($\overline{ERR}$) and shifted out in some of the serial modes when the SPI interface is selected.

**GLERR**
**Global Error Register**

**(Address : $04_H$)** **Reset Value: $06_H$**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | **0** | | | **UV** | **MV** | **CF** |
| | | r | | | | rh | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **CF** | 0 | rh | **Channel Fault**<br>This bit indicates that at least one wire-break condition has been detected at the channel inputs.<br>$0_B$ No wire-break condition has been detected at the channels .<br>$1_B$ At least one channel shows a wire-break condition . |
| **MV** | 1 | rh | **VBB Missing Voltage**<br>This bit indicates if a missing voltage condition has been detected at the VBB pin.<br>$0_B$ No missing voltage detected at VBB.<br>$1_B$ A missing voltage condition has been detected at VBB. |
| **UV** | 2 | rh | **VBB Under Voltage**<br>This bit indicates if an undervoltage condition has been detected at the VBB pin.<br>$0_B$ No undervoltage detected at VBB.<br>$1_B$ An undervoltage has been detected at VBB. |
| **0** | [7:3] | r | **Reserved**<br>returns 0 if read. |

### 6.3.4 Filter Time of Channel 0-7 Register

These registers define the filter time for both the data and diagnostics for each channel IN0-7. The wirebreak bit can additionally be masked in the **DIAG** register. These registers can be modified and read by the µController.

**COEFIL0-7**
**Channel 0-7 Filter Time Register**
**(Address : $06_H$ - $14_H$ for read access, $86_H$ - $94_H$ for write access )** **Reset Value: $1F_H$**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | MWB | FT | | | |
| | r | | rw | | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **FT** | [3:0] | rw | **Filter Time**<br>This bit field configures the filter time for averaging the Data and the Wire-Break signals detected at channels IN0-7.<br>$00_H$ 50 µs<br>$01_H$ 100 µs<br>$02_H$ 400 µs<br>$03_H$ 800 µs<br>$04_H$ 1,6 ms<br>$05_H$ 3,2 ms<br>$06_H$ 10 ms<br>$07_H$ 20 ms<br>$08_H$ - $0F_H$ bypassed (default) |
| **MWB** | 4 | rw | **Mask Wire-Break Detection**<br>This bit masks the filtered signal of the Wire-Break detection.<br>$0_B$ The wire-break signal is masked and is not visible in the **DIAG** register.<br>$1_B$ The wire-break signal is not masked and appears in the **DIAG** register. (default). |
| **0** | [7:5] | r | **Reserved**<br>returns 0 if read; should be written with 0. |

### 6.3.5 Internal Error Register

This register contains the status of the internal errors monitored for safe IC operation. The bits are sticky and remain set once the fault condition is detected until a read operation occurs and the faults are resolved. The bits of the **INTERR** register are used in the generation of the signal of the error pin ($\overline{ERR}$) and shifted out in some of the serial modes when the SPI interface is selected. On power up (UVLO), the bits W4S and TE are preset to High and will have to be cleared by a read access during the startup phase.

**INTERR**
**IC Status Register**

**(Address : $16_H$)** **Reset Value: $06_H$**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | **0** | | | **W4S** | **TE** | **DC_ERR** |
| | | r | | | | rh | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **DC_ERR** | 0 | rh | **DC-DC Converter Error**<br>This bit indicates if overload condition has been detected at the SW1 or SW2 switches.<br>$0_B$ No overload detected.<br>$1_B$ Overload detected. |
| **TE** | 1 | rh | **Transmission Error**<br>This bit indicates if a transmission error has been detected over the Coreless Transformer between the Sense side chip and the µController side chip.<br>$0_B$ No transmission error.<br>$1_B$ Transmission error. |
| **W4S** | 2 | rh | **Wait for Sense Chip**<br>This bit indicates the Sense side chip is correctly supplied and ready for transmission.<br>$0_B$ Sense Side is ready.<br>$1_B$ Sense Side is not ready because of insufficient supply or long transmission error. |
| **0** | [7:3] | r | **Reserved**<br>returns 0 if read. |

### 6.3.6 Global Configuration Register

This register contains configuration parameters for the sensor type selection as well as the DC-DC driver.

**GLCFG**

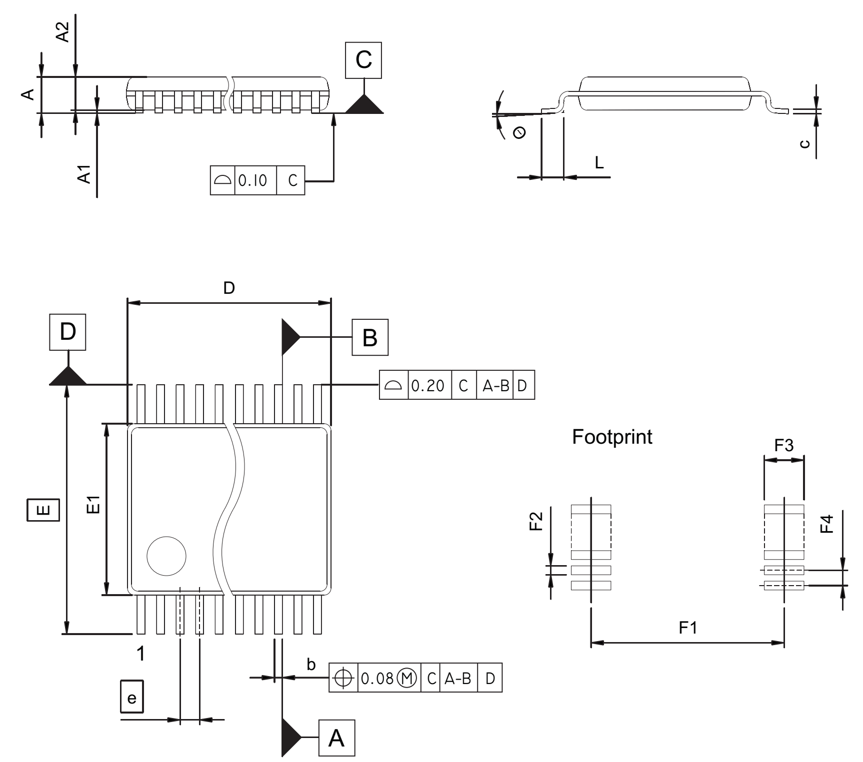
**Global Configuration Register**

**(Address : $18_H$ for read access, $98_H$ for write access, )** **Reset Value: $00_H$**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | **0** | | **DIAG ACLR** | **SW_RST** | **DCK** | **0** | |
| | r | | rw | rw | rw | r | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **0** | 1:0 | rw | **Reserved**<br>returns 0 if read; should be written with 0. |
| **DCK** | 2 | rw | **DC-DC Driver Switching Frequency Ratio**<br>This bit indicates the ratio between the sampling clock frequency set at Rosc and the switching frequency of the DC-DC driver (pins SW1/2).<br>$0_B$ DC-DC switching frequency is equal to the sampling frequency (1:1) (default).<br>$1_B$ DC-DC switching frequency is half to the sampling frequency (2:1). |
| **SW_RST** | 3 | rw | **Soft-Reset for the Filtering Stage**<br>This bit triggers the reset of the Filter registers<br>$0_B$ No Reset<br>$1_B$ Reset is generated for the Filter stage |
| **DIAG_ACLR** | 4 | rw | **Diagnostics Automatical Clear**<br>This bit selects if the **DIAG** register is automatically cleared after any access to the **DIAG** register (especially for the second SPI channel at the SSO pin, see **Table 6-3**). The diagnostics remain in both case sticky.<br>$0_B$ Automatical clear after any access to the **DIAG** register (default)<br>$1_B$ Automatical clear disabled |
| **0** | [7:5] | r | **Reserved**<br>returns 0 if read; should be written with 0. |

# 7 Package Outline




1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | - | 1.10 | - | 0.043 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.80 | 1.05 | 0.031 | 0.041 |
| b | 0.17 | 0.27 | 0.007 | 0.011 |
| c | 0.09 | 0.16 | 0.004 | 0.006 |
| D | 12.40 | 12.60 | 0.488 | 0.496 |
| E | 8.10 BSC | | 0.319 BSC | |
| E1 | 6.00 | 6.20 | 0.236 | 0.244 |
| e | 0.50 BSC | | 0.020 BSC | |
| N | 48 | | 48 | |
| L | 0.50 | 0.75 | 0.020 | 0.030 |
| Θ | 0° | 8° | 0° | 8° |
| F1 | 7.80 | | 0.307 | |
| F2 | 0.29 | | 0.011 | |
| F3 | 1.30 | | 0.051 | |
| F4 | 0.50 | | 0.020 | |

DOCUMENT NO.
Z8B00158954

SCALE 0 1.0 2mm

EUROPEAN PROJECTION

ISSUE DATE
14.06.2011

REVISION
03

**Figure 7-1 Package Outline TSSOP-48 (tie bar not drawn in outline)**

**Notes**

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Packages":* ***http://www.infineon.com/packages***
2. *Dimensions in mm.*

w w w . i n f i n e o n . c o m

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